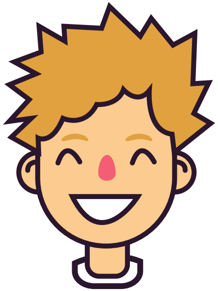
# Another Flip in the Row

Daniel Gruss, Moritz Lipp, Michael Schwarz

August 9, 2018

Graz University of Technology

## Who am I?



**Daniel Gruss**

PostDoc @ Graz University of Technology

@lavados

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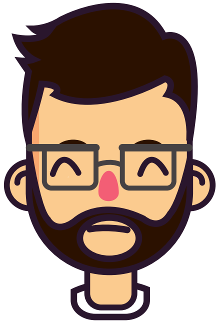

**Moritz Lipp**

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moritz.lipp@iaik.tugraz.at

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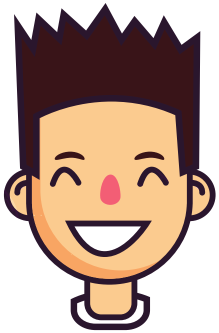

**Michael Schwarz**

PhD student @ Graz University of Technology

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## And the rest of the team

The rest of the research team

- Clémentine Maurice
- Daniel Genkin
- Jonas Juffinger
- Lukas Raab
- Lukas Lamster
- Misiker Tadesse Aga
- Sioli O’Connell
- Wolfgang Schoechl
- Yuval Yarom

## DRAM organization

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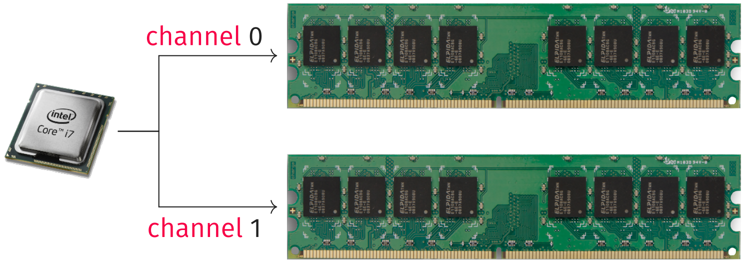

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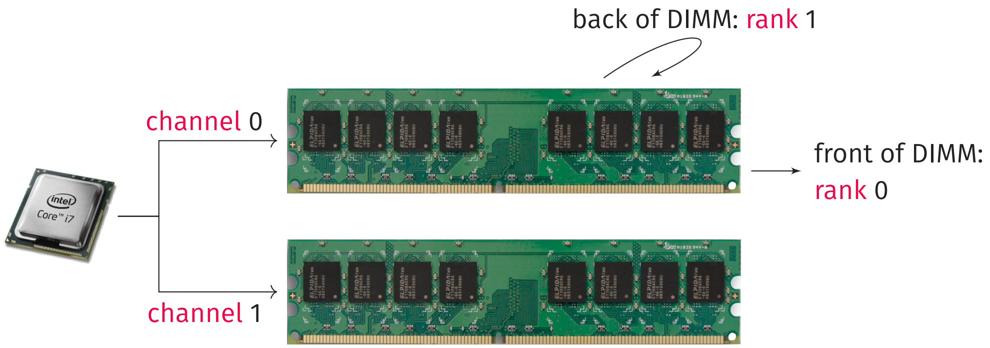

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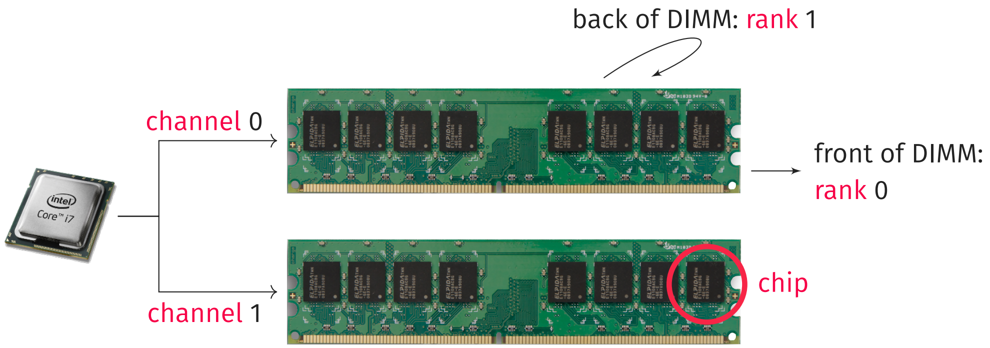
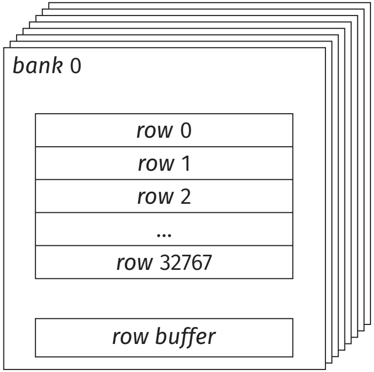


## DRAM organization

*chip*



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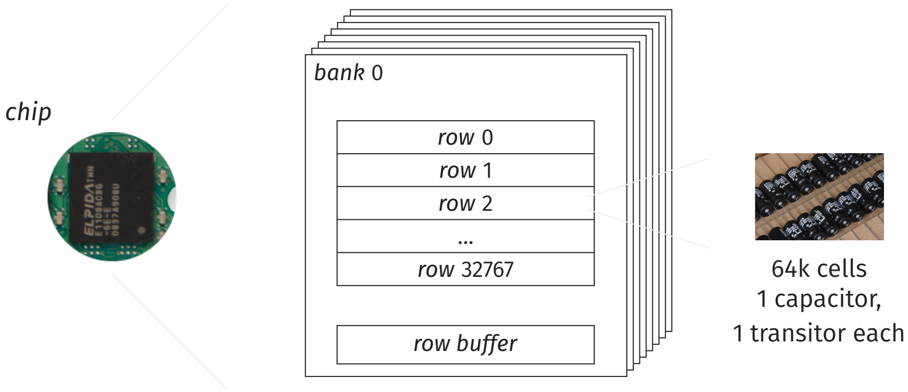
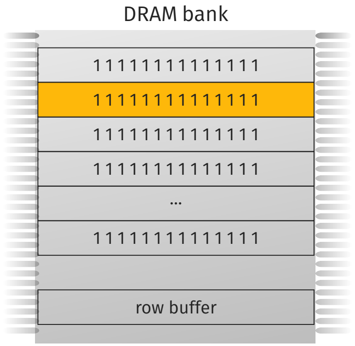


# How reading from DRAM works



CPU wants to access row 1

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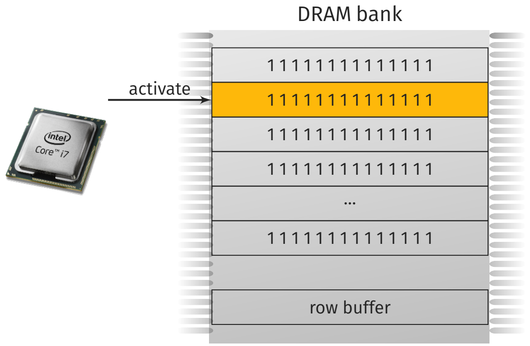

CPU wants to access row 1

$\rightarrow$ row 1 activated

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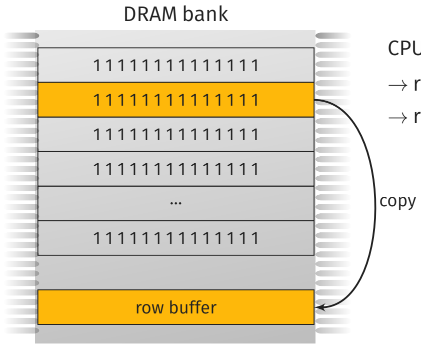

CPU wants to access row 1

→ row 1 activated

→ row 1 copied to row buffer

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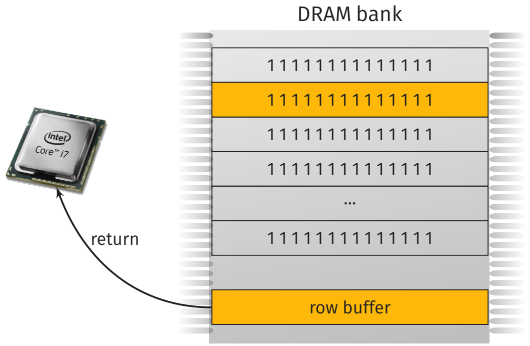

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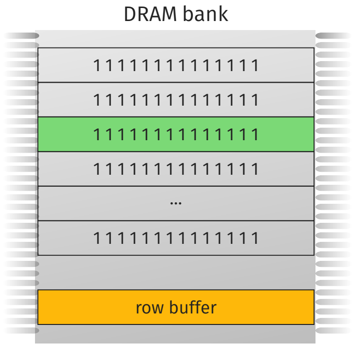

CPU wants to access row 2

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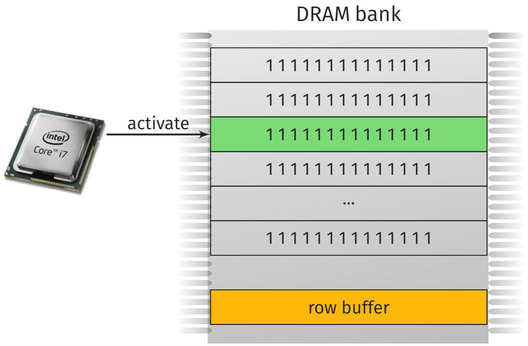

CPU wants to access row 2

$\rightarrow$ row 2 activated

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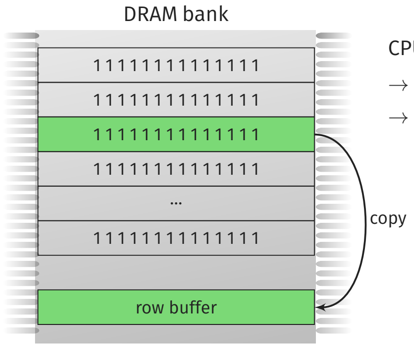

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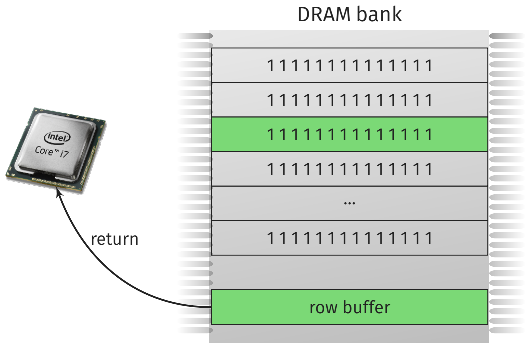

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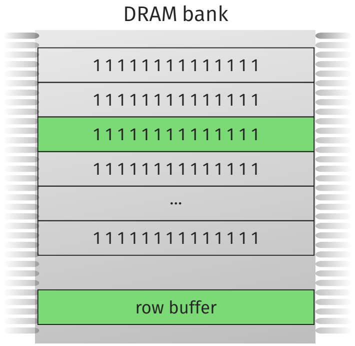


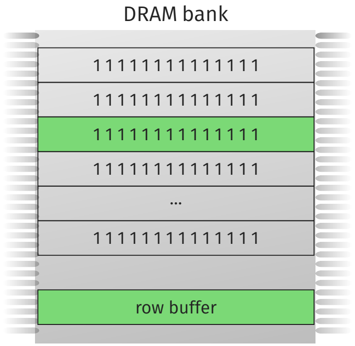
CPU wants to access row 2

→ row 2 activated

→ row 2 copied to row buffer

→ slow (row conflict)

## How reading from DRAM works



CPU wants to access row 2—again

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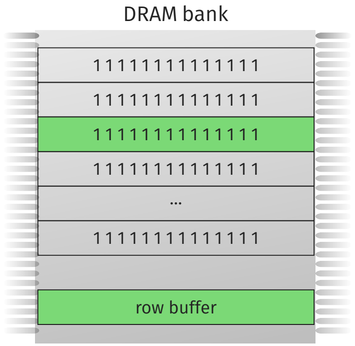

CPU wants to access row 2—again

$\rightarrow$ row 2 already in row buffer

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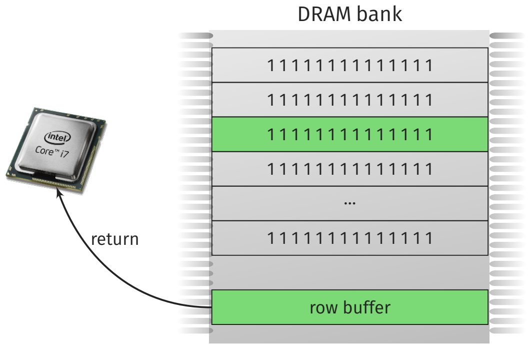

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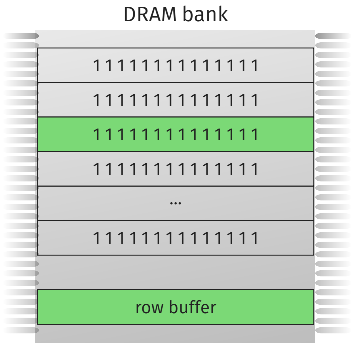

CPU wants to access row 2—again

→ row 2 already in row buffer

→ fast (row hit)

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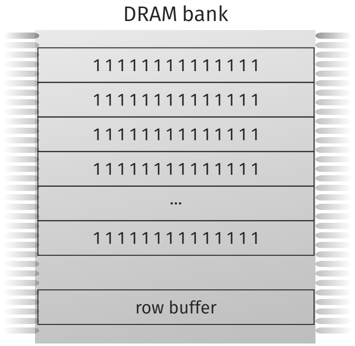
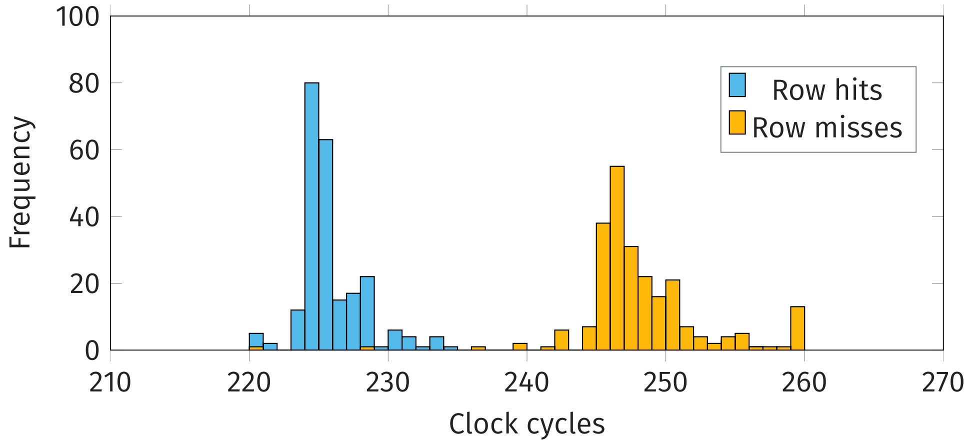
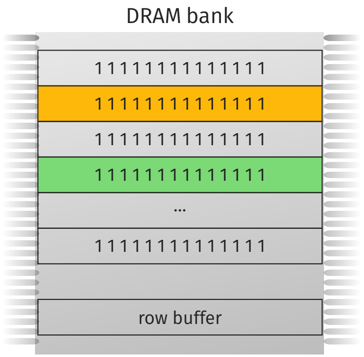


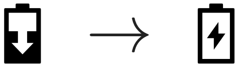
**row buffer = cache**

## Timing difference



## Rowhammer


DRAM bank
1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1
...
1 1 1 1 1 1 1 1 1 1 1 1 1 1
row buffer



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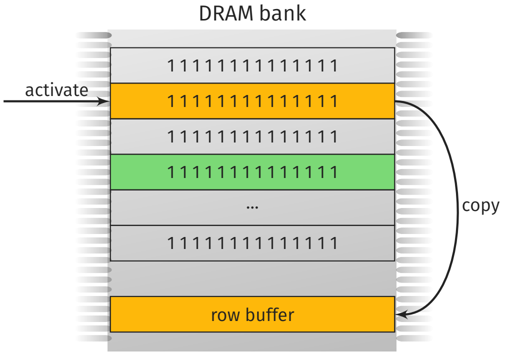
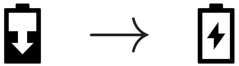

DRAM bank
activate
1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1
...
1 1 1 1 1 1 1 1 1 1 1 1 1 1
row buffer
copy



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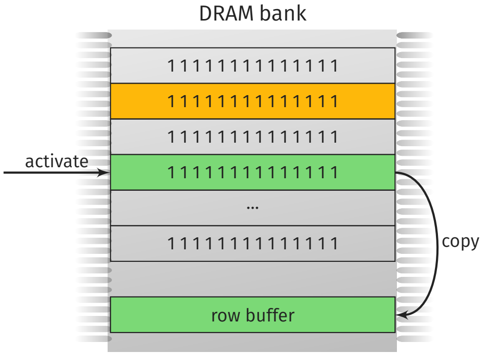

Cells leak faster upon proximate accesses → Rowhammer

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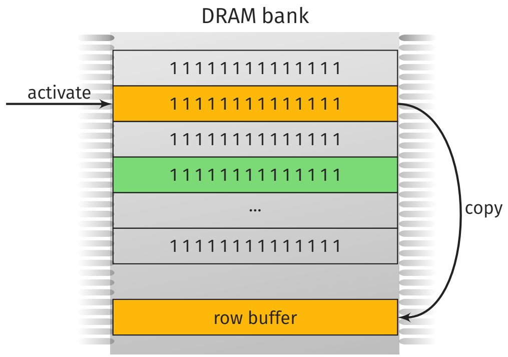

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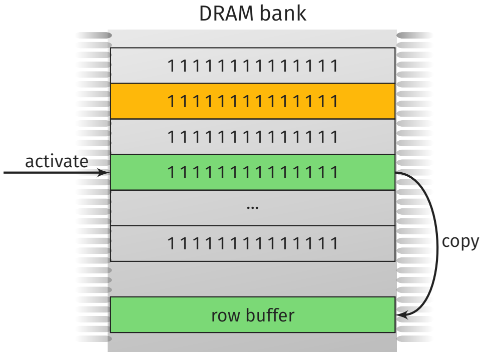

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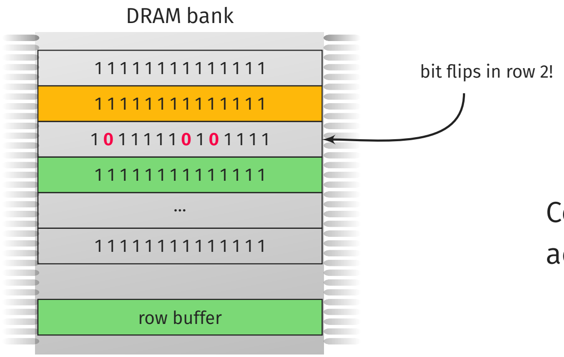

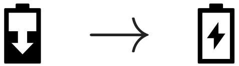

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DDR4

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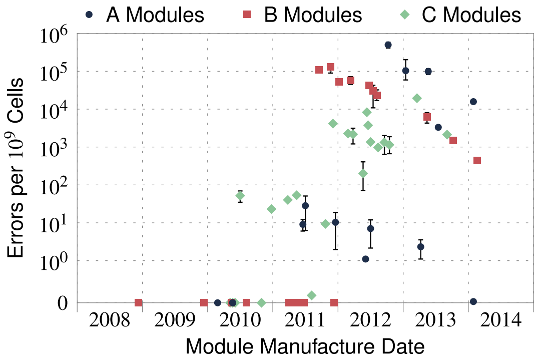

BIT FLIPS
BIT FLIPS EVERYWHERE

## Requirements

Memory accesses must be

- uncached: reach DRAM
- fast: race against the next row refresh
- targeted: reach specific row

## How do we get enough uncached accesses?

## Access techniques

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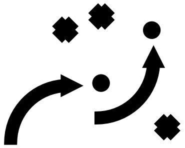

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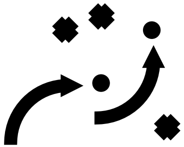

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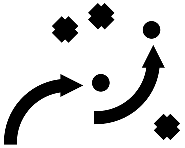

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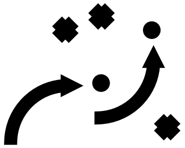

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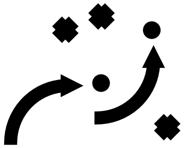

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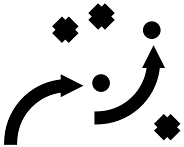

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- cache eviction [GMM16; Awe+16]
- non-temporal accesses [QS16]
- uncached memory [Vee+16]

## How do we target accesses?

## Physical addresses and DRAM

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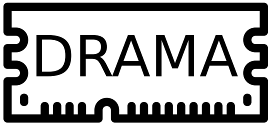

## Physical addresses and DRAM

**DRAMA: How your DRAM becomes a security problem**

Anders Fogh & Michael Schwarz

Black Hat Europe 2016

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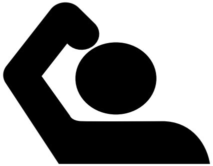

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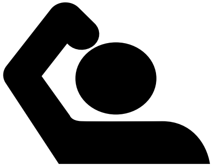

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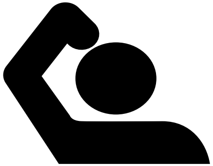

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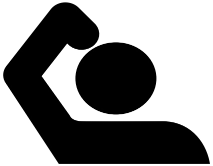

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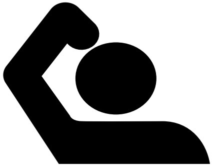

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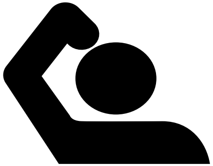

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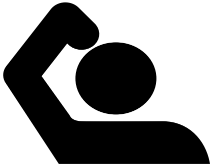

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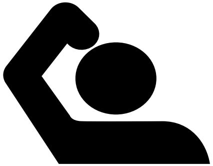

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- Alternatively: Build a PUF [Ana+18]

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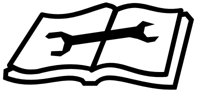

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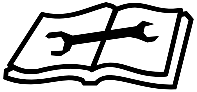

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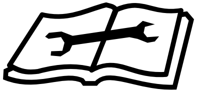

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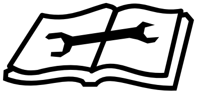

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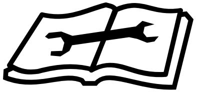

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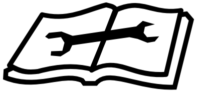

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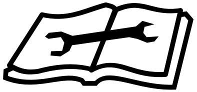

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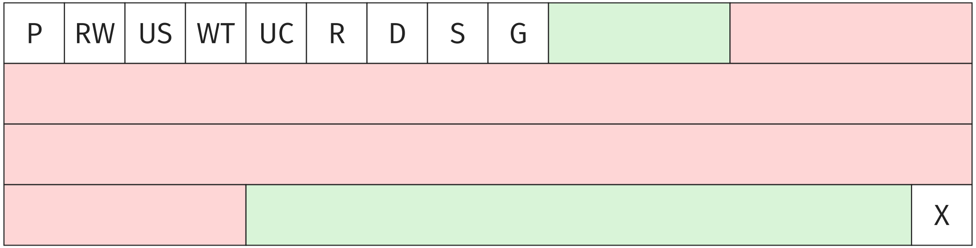
- Flip a bit in a validated NaCl instruction sequence
  - Safe + validated jump $\rightarrow$ arbitrary jump

## Page Table Entries



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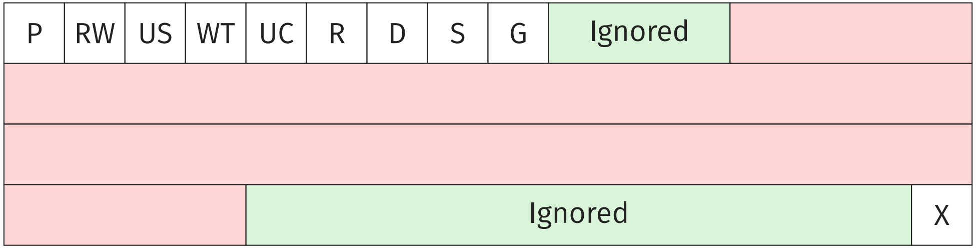

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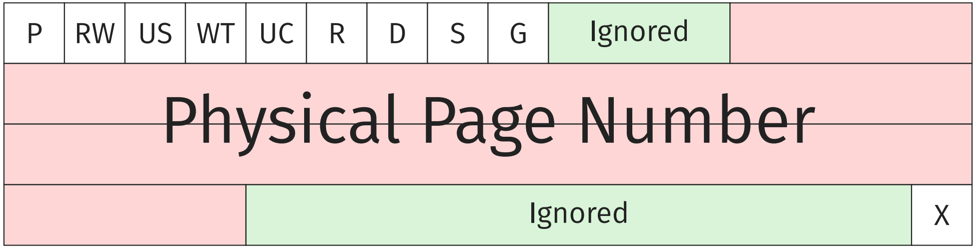

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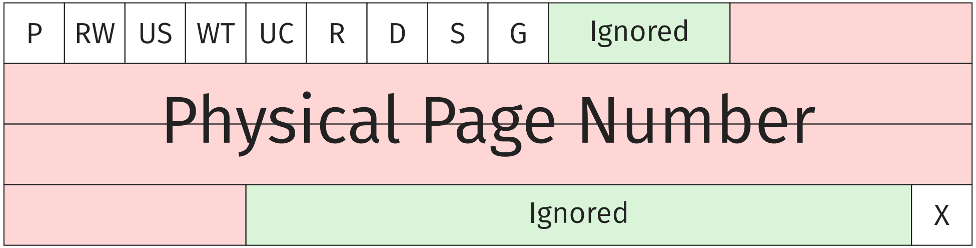
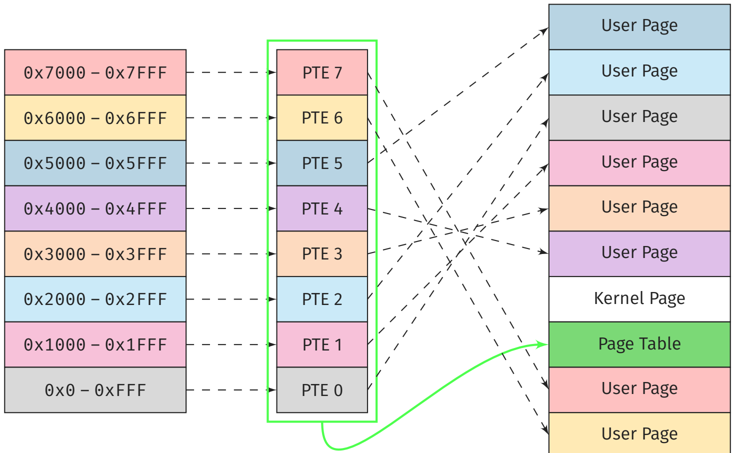


Each 4 KB page table consists of 512 such entries

## Page Table Manipulation



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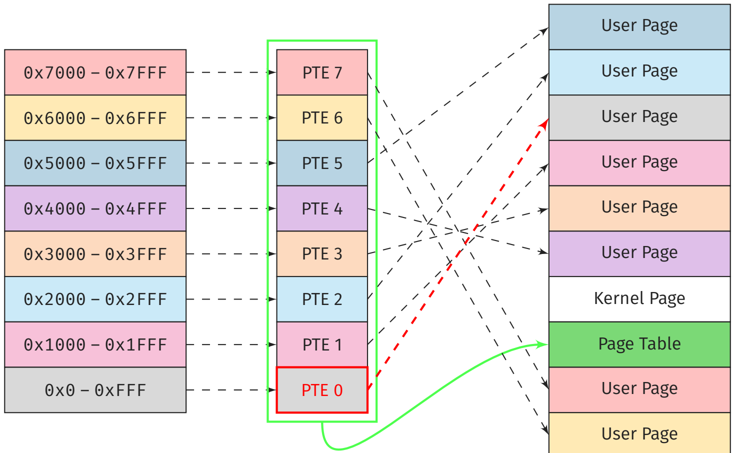

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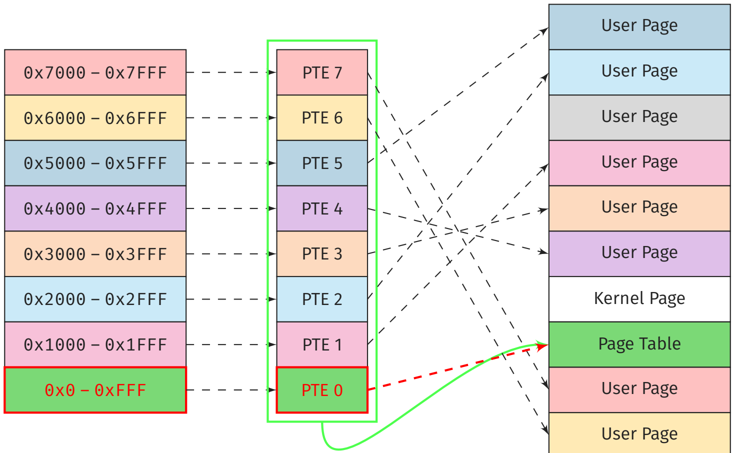

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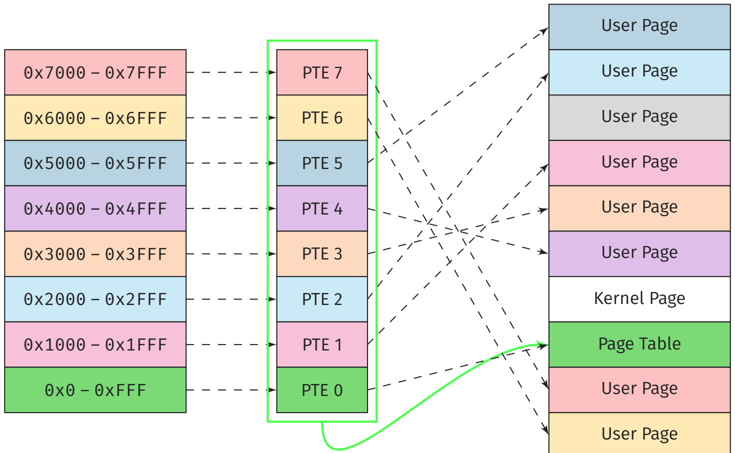

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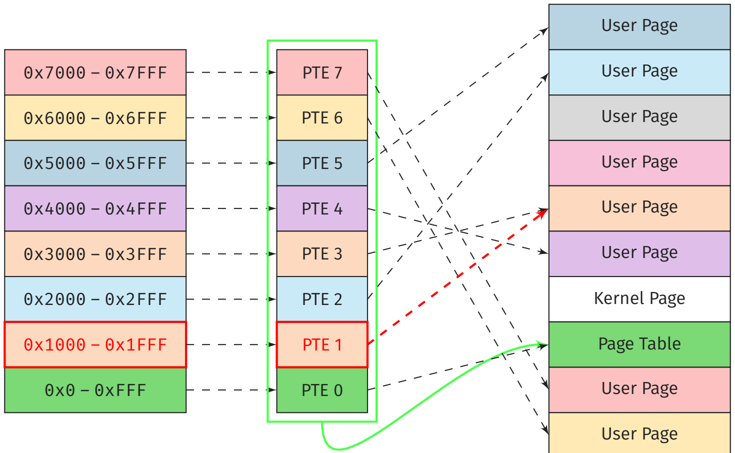

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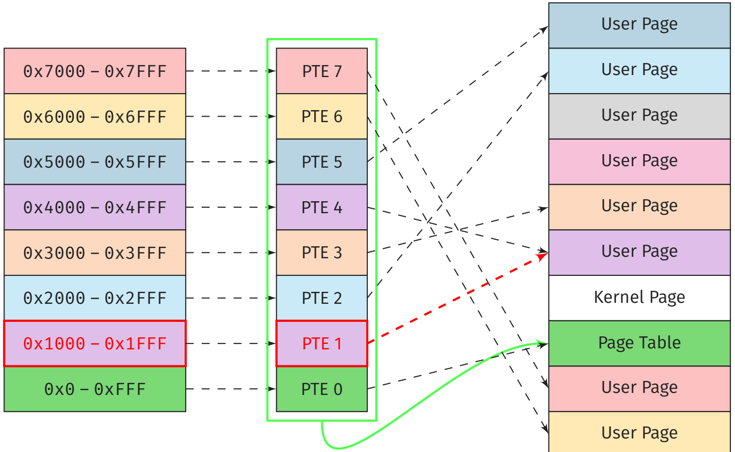

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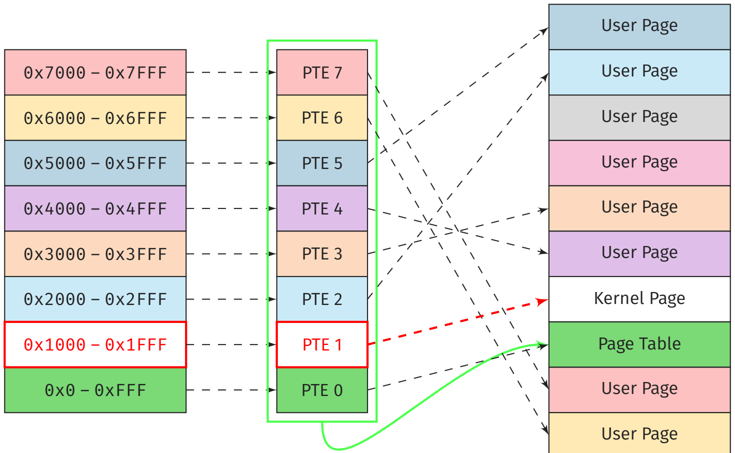
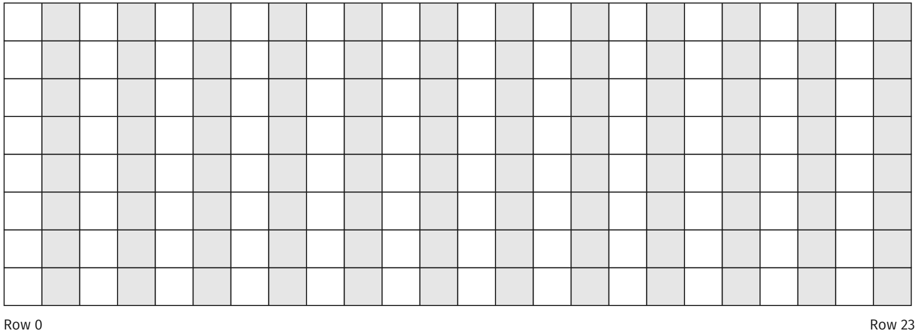


## Search for page with flip



Hammering memory locations in different rows

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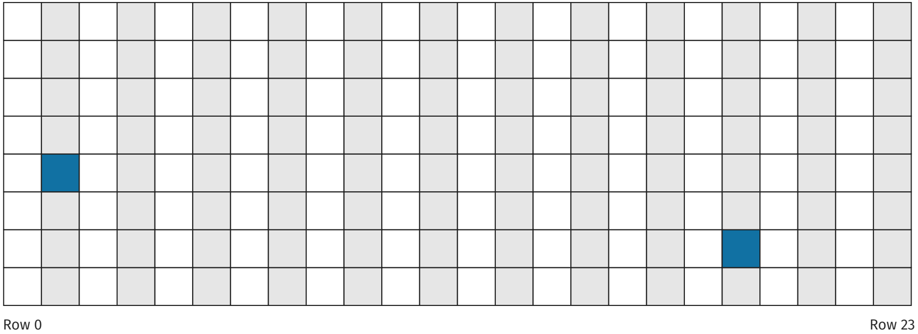

Hammering memory locations in different rows

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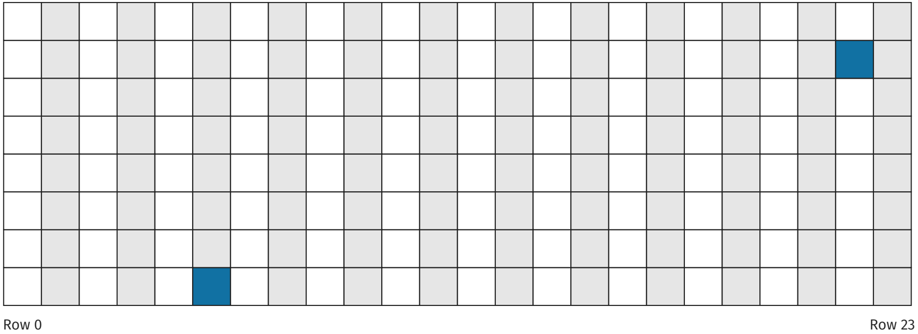

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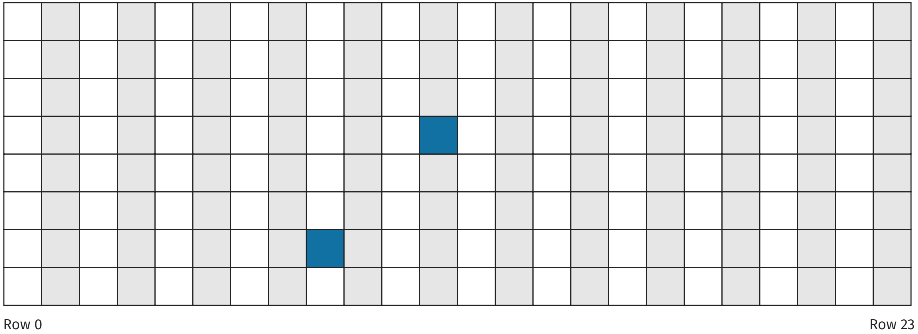

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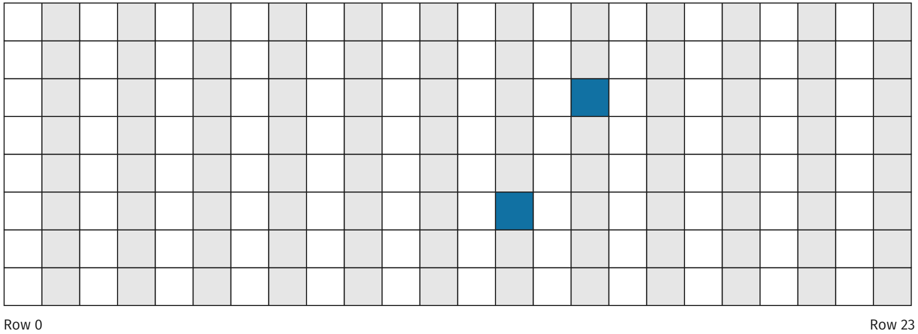

Hammering memory locations in different rows

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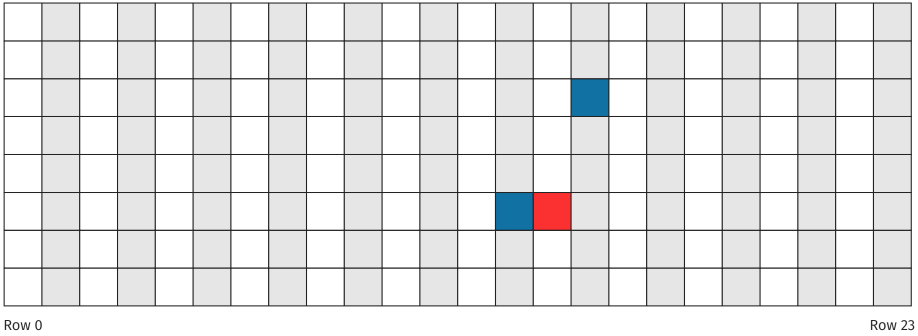
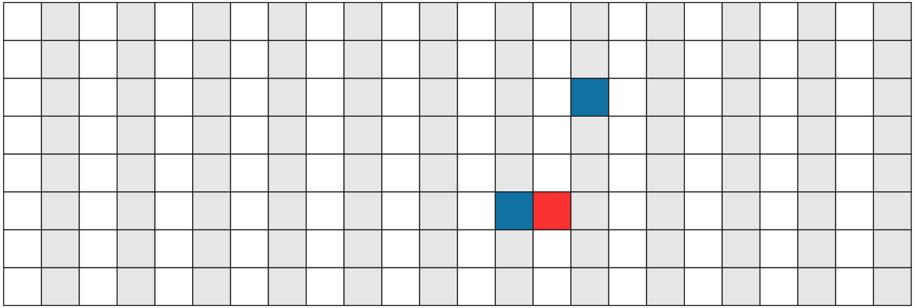
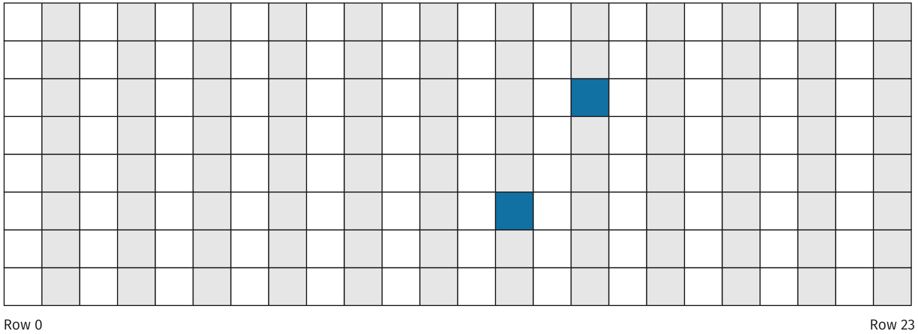


Hammering memory locations in different rows

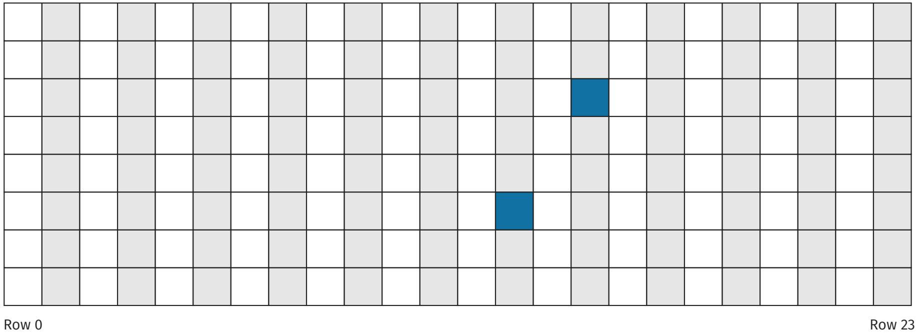
## Release page with flip



## Release page with flip



## Fill all remaining memory with page tables



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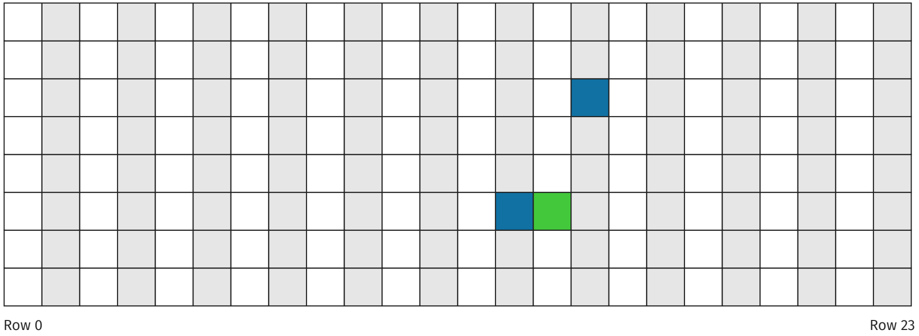

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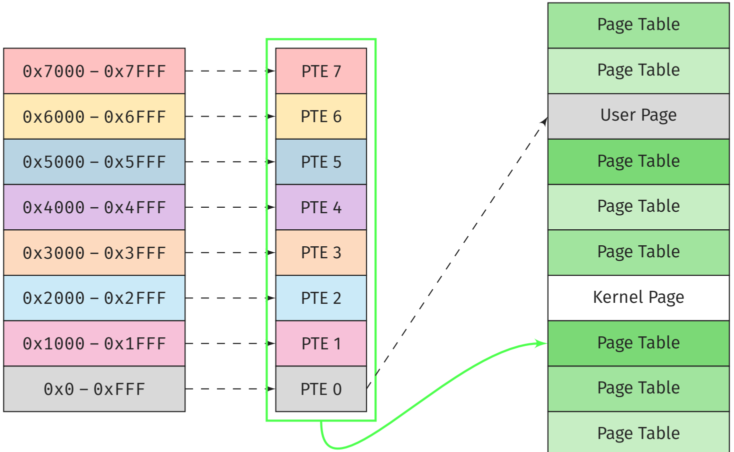

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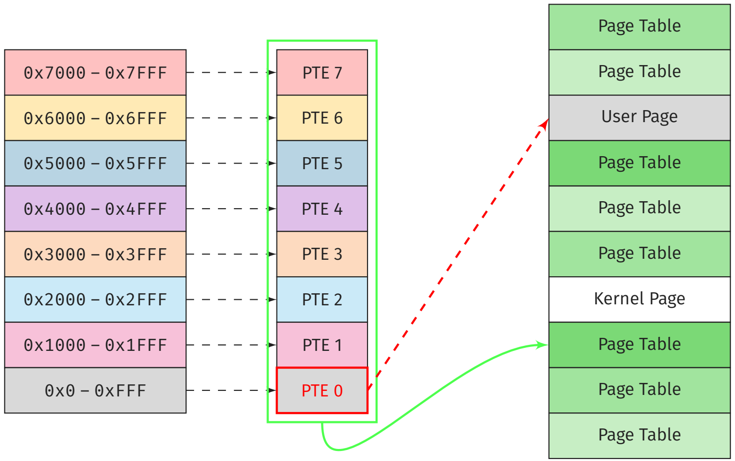

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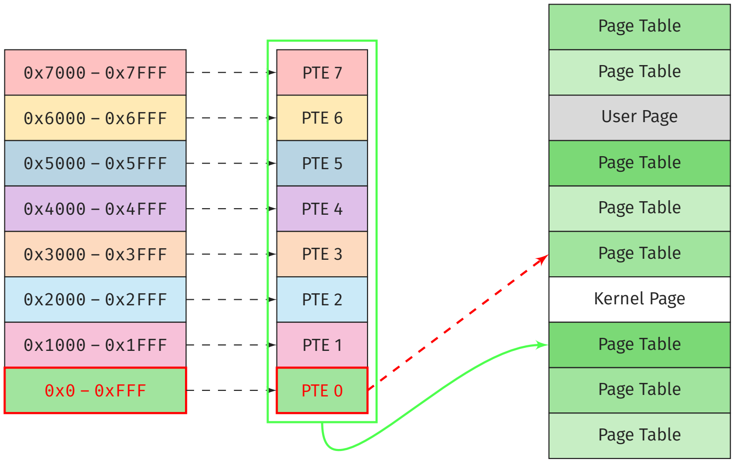

## Strategy: Flipping Page Table PPN bits

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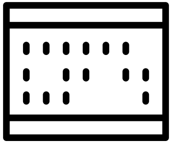

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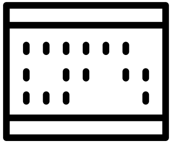

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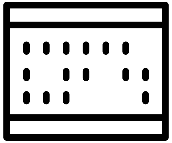

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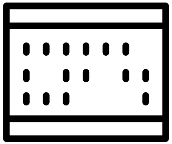

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## Strategy: Flipping Page Table PPN bits

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3. Gain access to your own page table $\rightarrow$ kernel privileges

## Flipping Page Table PPN bits

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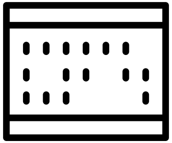

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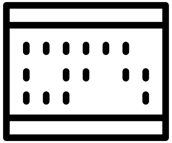

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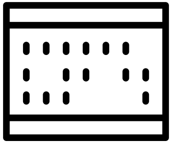

- Idea from [SD15]

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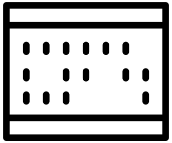

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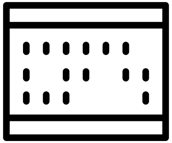

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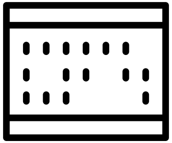

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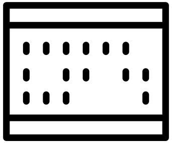

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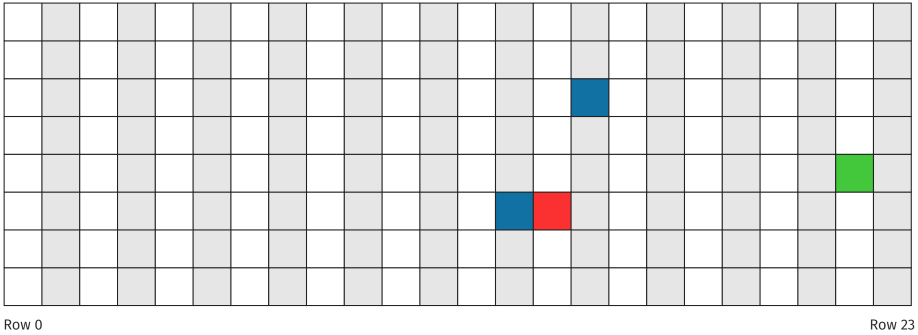
  - etc.
- pages are pretty unique: 32768 bits per page

## Bit Flips + Page Deduplication



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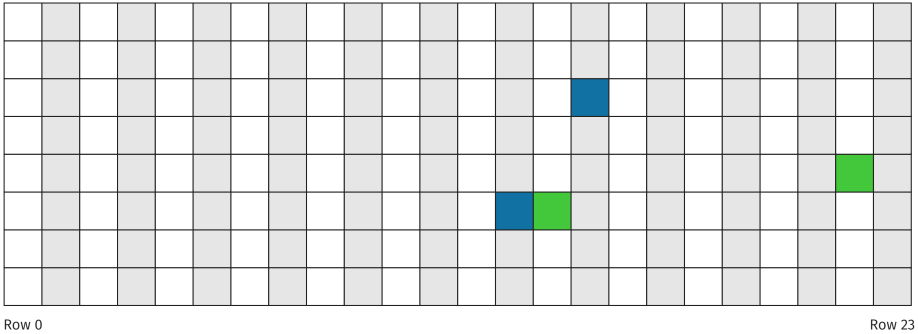
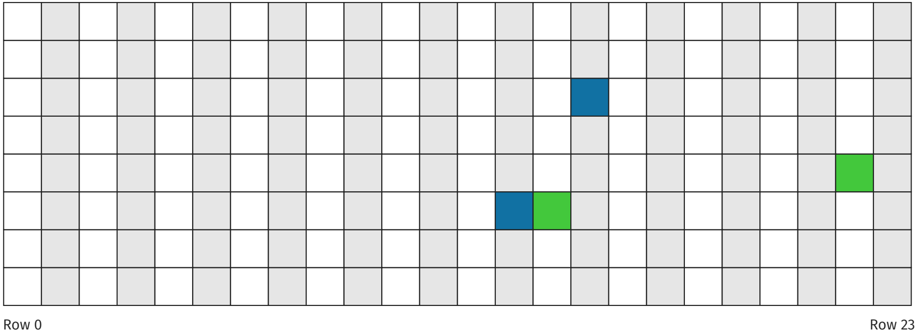


Page with bit flip is filled with target content

## Bit Flips + Page Deduplication



OS or hypervisor searches for duplicate pages

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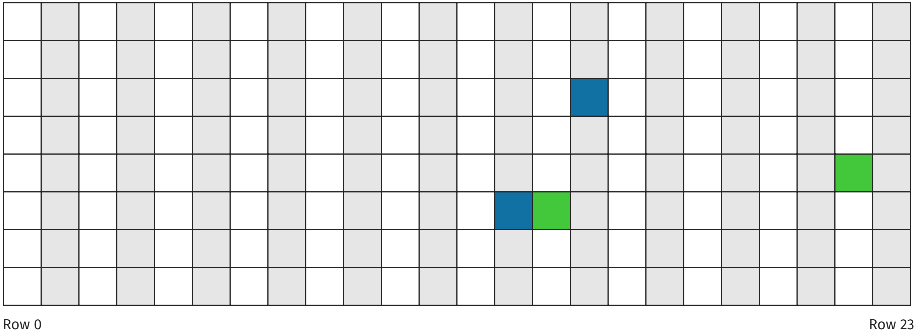

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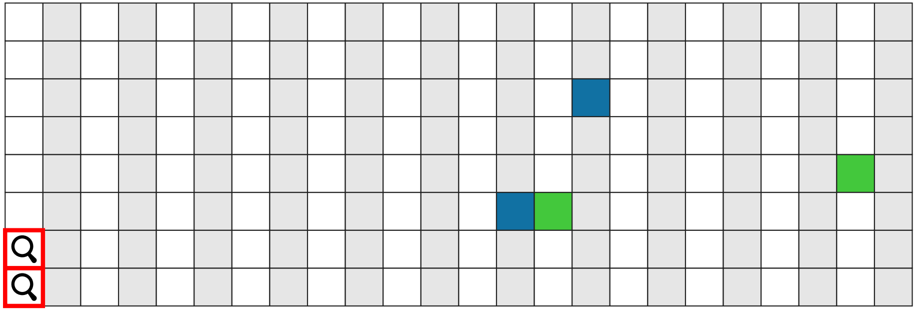

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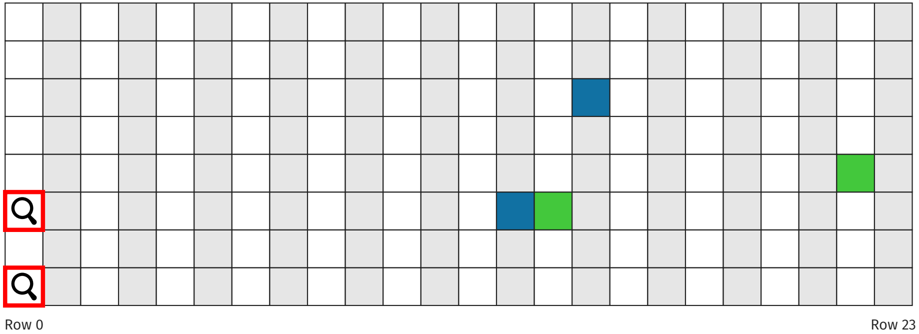

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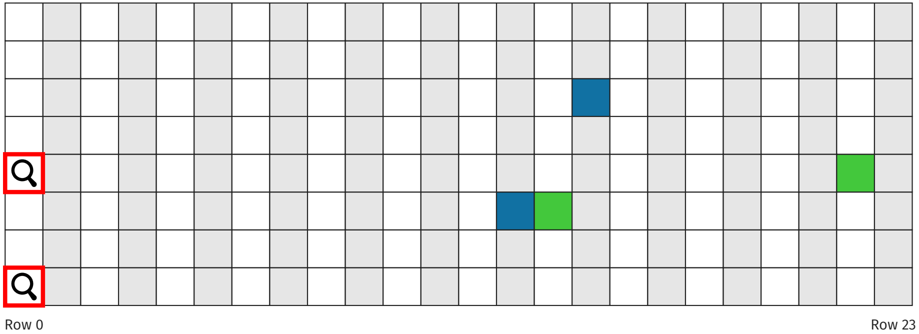

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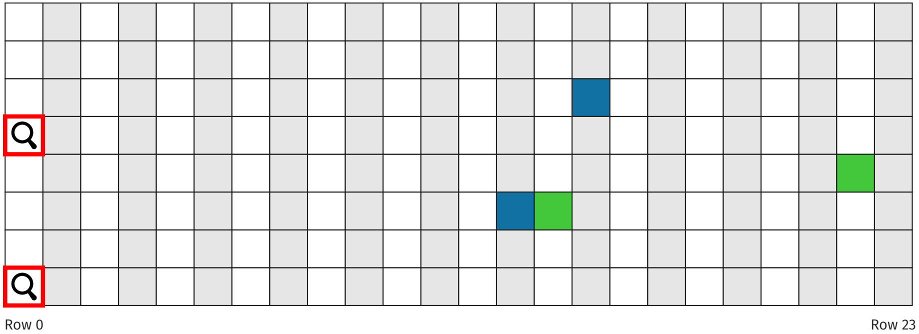

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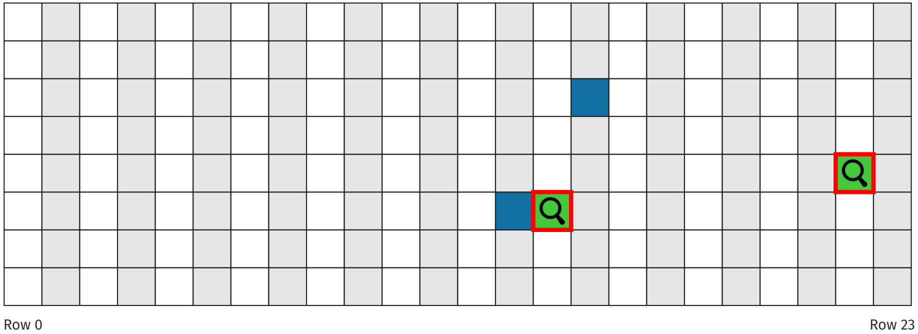

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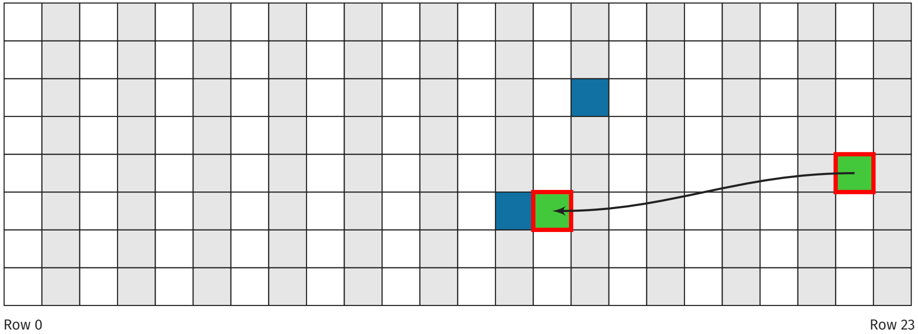

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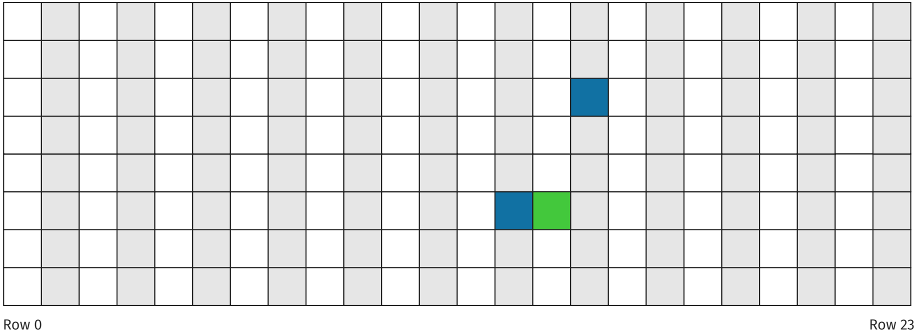
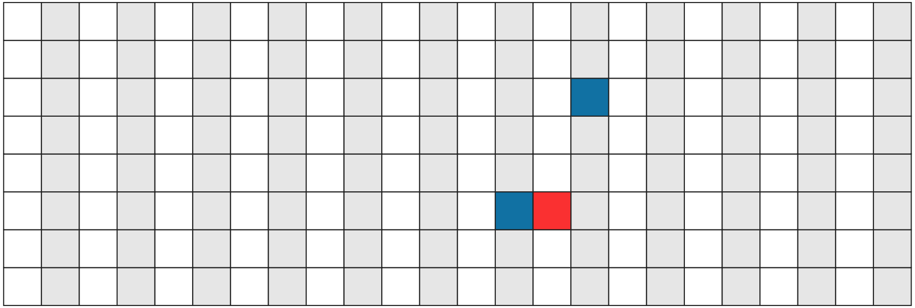


Hammer again + flip again

# Bit Flips + Page Deduplication


Row 0

Row 23

## Strategy: Flipping in Deduplicated Pages

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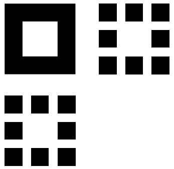

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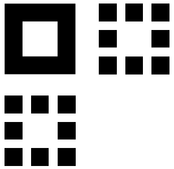

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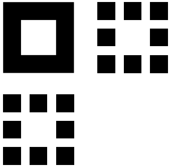

1. Scan for flips

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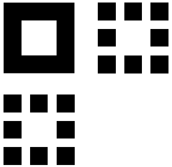

1. Scan for flips
2. Place content for deduplication so that flip can be exploited

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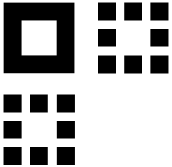

1. Scan for flips
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3. Perform the bit change through Rowhammer

## Flipping in Deduplicated Pages

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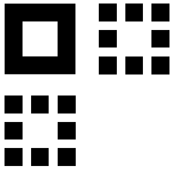

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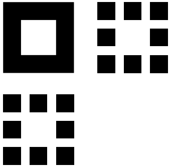

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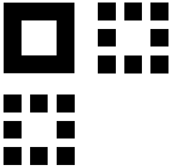

- Idea from [Bos+16]

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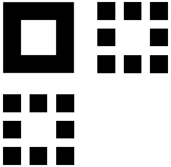

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  - Change data type (double $\rightarrow$ pointer)

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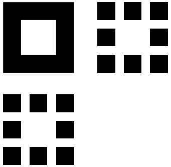

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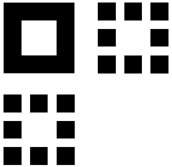
# Flipping in Deduplicated Pages



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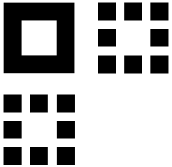
- and from [Raz+16]

## Flipping in Deduplicated Pages



- Idea from [Bos+16]
    - Change data type (double $\rightarrow$ pointer)
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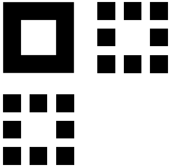
## Flipping in Deduplicated Pages



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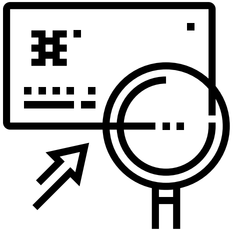
## How to mitigate Rowhammer?

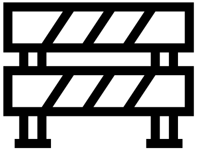
## Mitigations

Different mitigations have been proposed:



Detection

vs



Prevention

## Mitigations

Different mitigations have been proposed:

Software

**vs**

Hardware

## Mitigations

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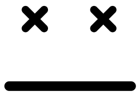
Short Term

**vs**

Long Term

## Quick fixes

- No `clflush` instruction



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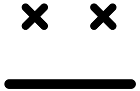

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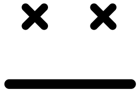

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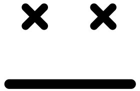

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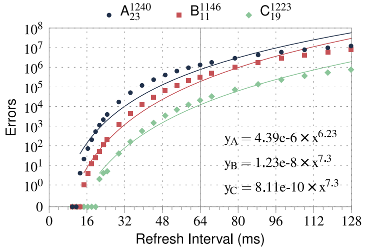

Errors depending on refresh interval [Kim+14]

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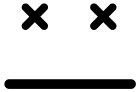

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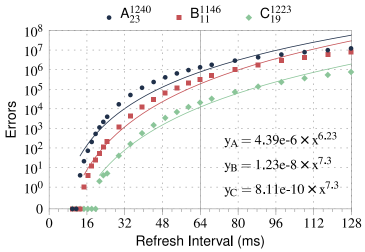

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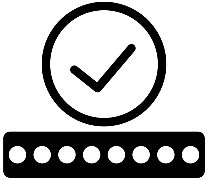

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→ Expensive, performance overhead, or increased power consumption

## Preventing Rowhammer attacks in hardware (2/3)

PARA - Probabilistic Adjacent Row Activation [Kim+14]

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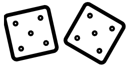

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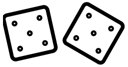

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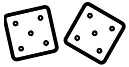

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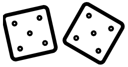

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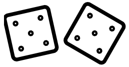

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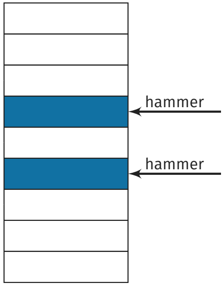

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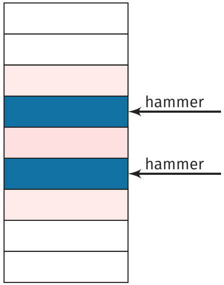

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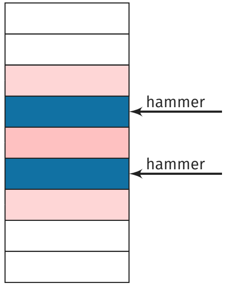

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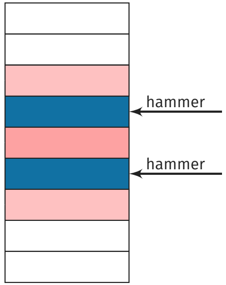

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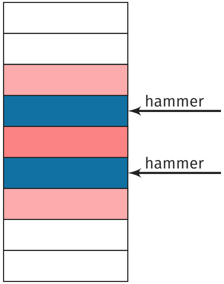

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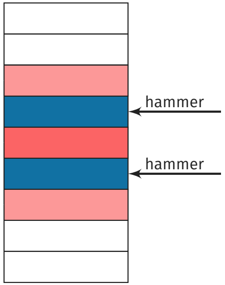

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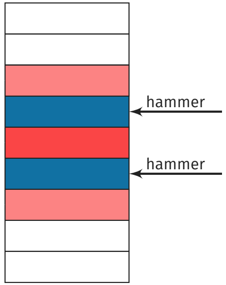

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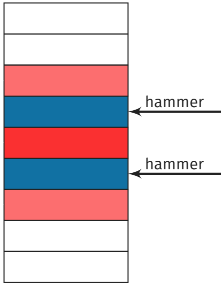

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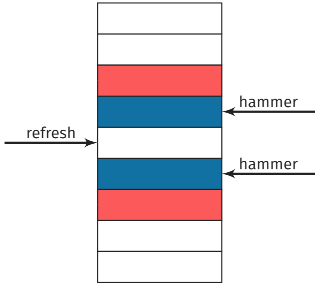

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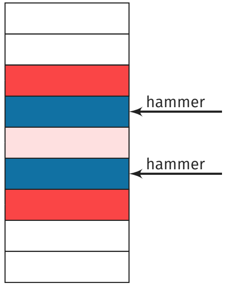

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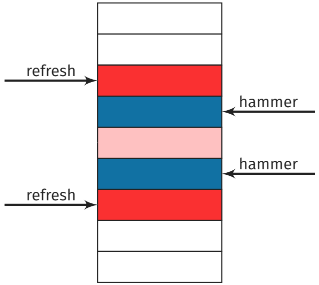

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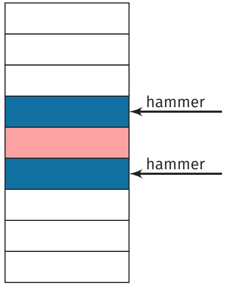

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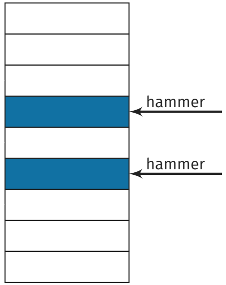

We flipped bits on DDR4 with TRR activated!

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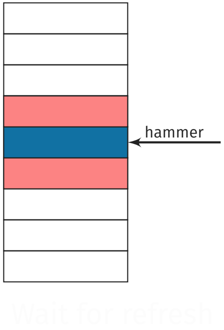

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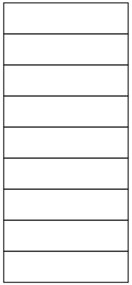

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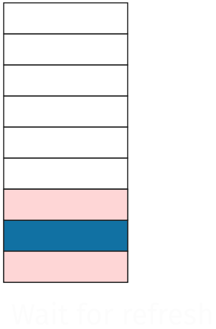

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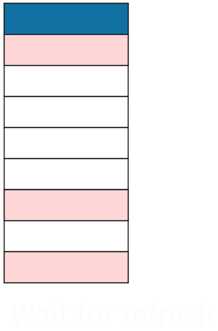

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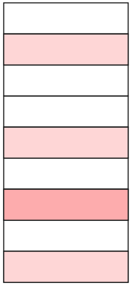

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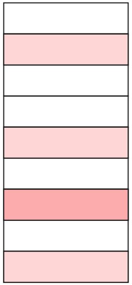

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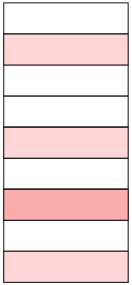

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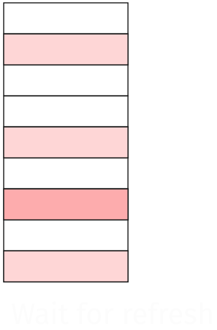

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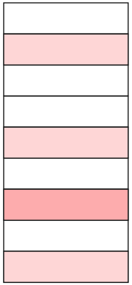

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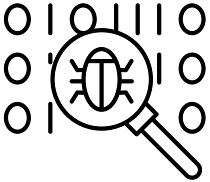

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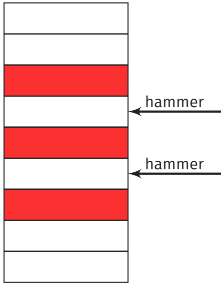

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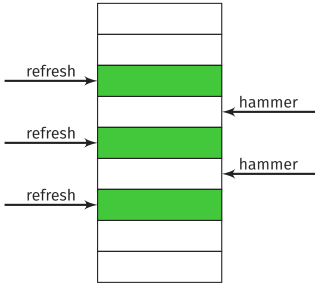

What if performance counters do not work? [Gru+18; Jan+17]

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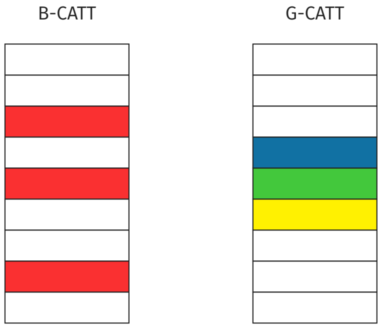

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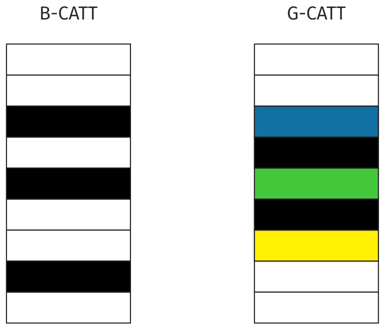

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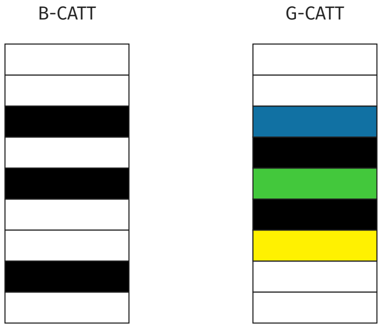

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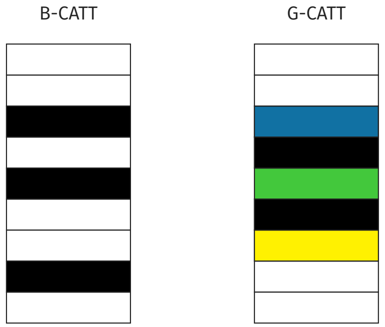

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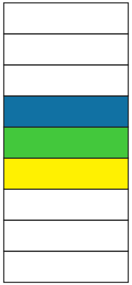

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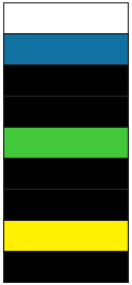

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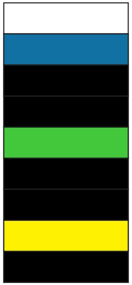

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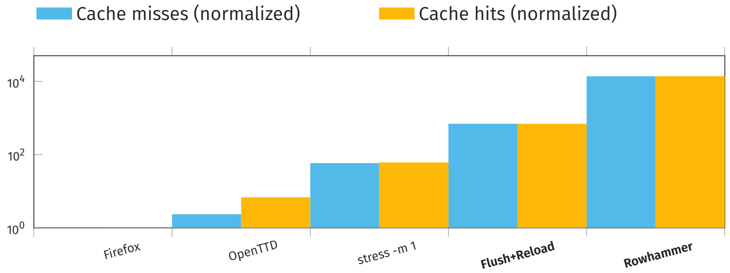

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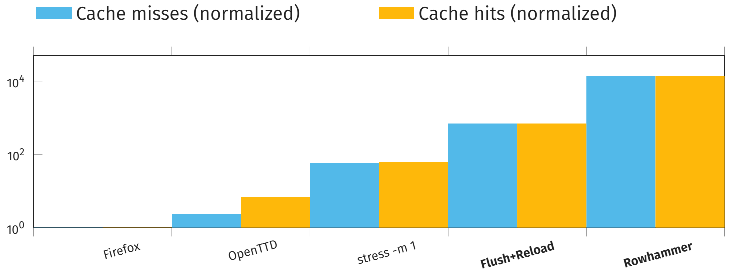

What if performance counters do not work because we run in SGX? [Gru+18; Jan+17]

## Defenses Overview

| Methodology \ Defense | MASCAT | Chiapetta et al. [CSY15] | CloudRadar | Herath and Fogh [HF15] | HexPADS | perf | ANVIL | nohammer | No OOM | G-CATT | B-CATT | TRR | MAC | PARA/CRA/PRA | ARMOR | ECC/Chipkill | Refresh Rate |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Detection** | | | | | | | | | | | | | | | | | |
| Static Analysis | ● | ○ | ○ | ◐ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| Performance Counters | ○ | ● | ● | ● | ● | ● | ● | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| Memory Access Pattern | ○ | ○ | ○ | ○ | ○ | ○ | ● | ● | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| **Neutralization** | | | | | | | | | | | | | | | | | |
| Physical Proximity | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ● | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| Memory Footprint | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ● | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| **Elimination** | | | | | | | | | | | | | | | | | |
| Bootloader | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ● | ○ | ○ | ○ | ○ | ○ | ○ |
| Hardware Modification | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ● | ● | ● | ● | ● | ○ |
| BIOS Update | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ● |

## What if you don’t need to hammer two or more rows?

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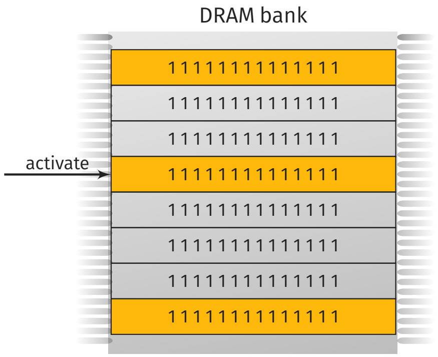

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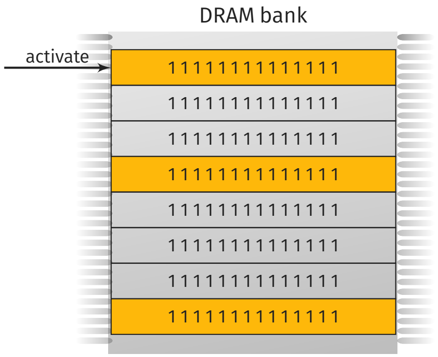

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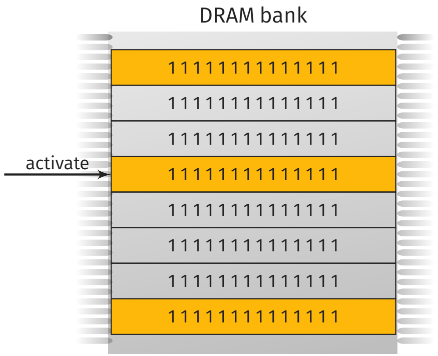

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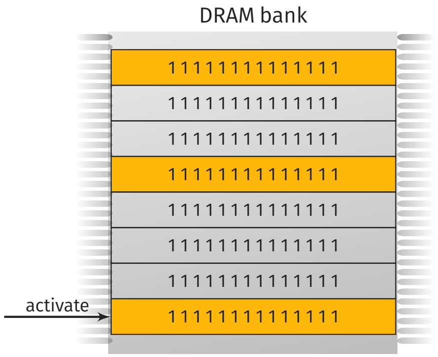

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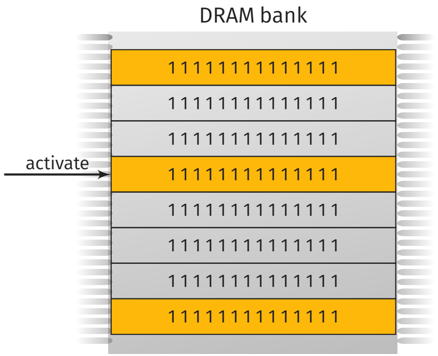

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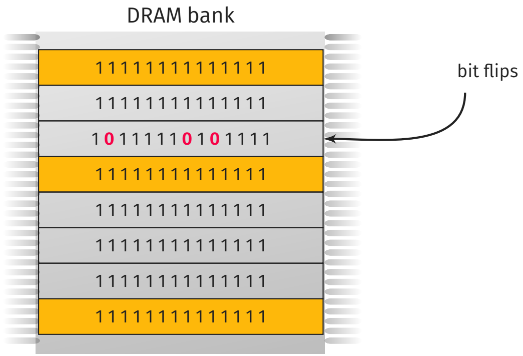

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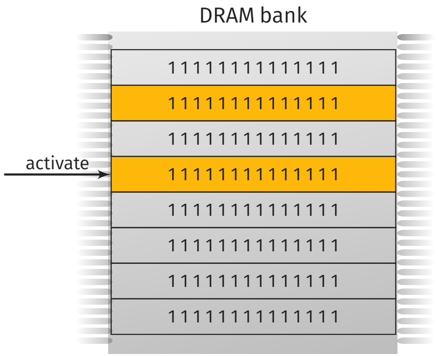

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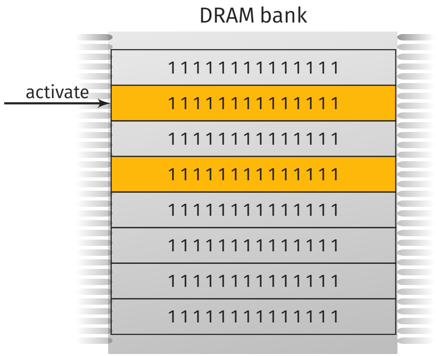

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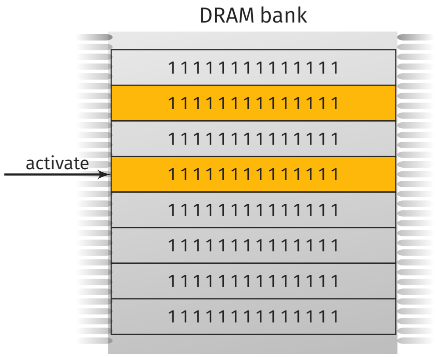

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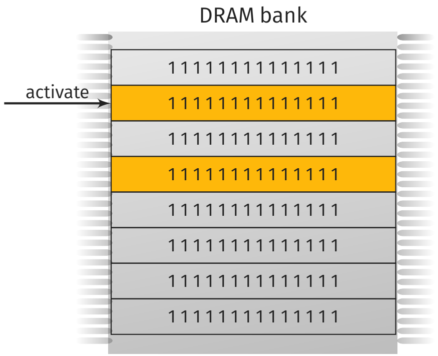

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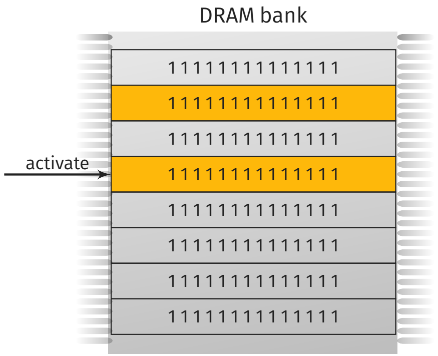

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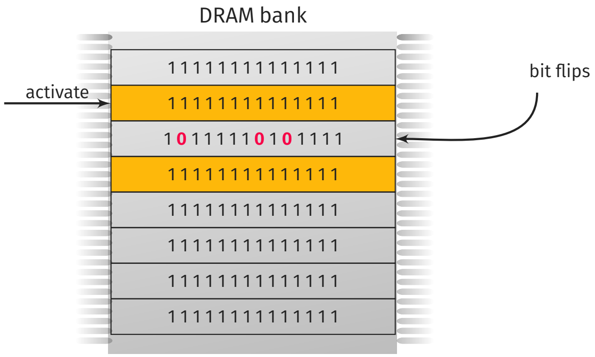
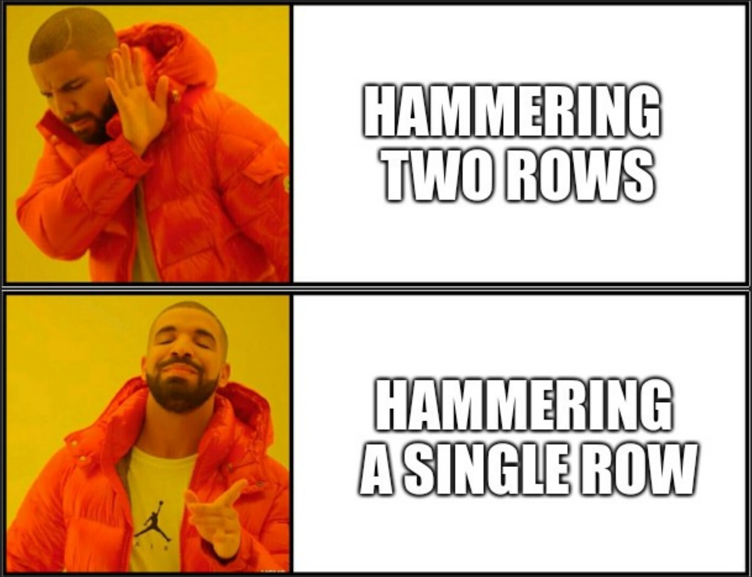
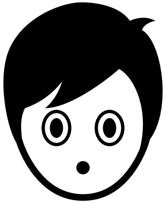


HAMMERING TWO ROWS


HAMMERING TWO ROWS
HAMMERING A SINGLE ROW

## Hammering techniques



- There are three different hammering techniques
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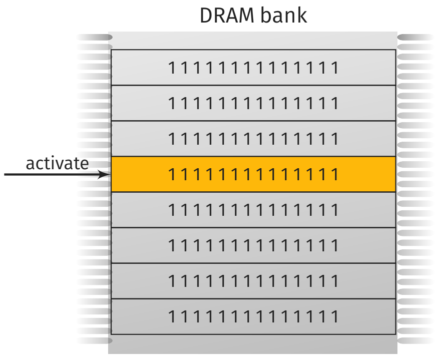
- #3: Hammer only one row next to victim row

## #3 - One-location hammering



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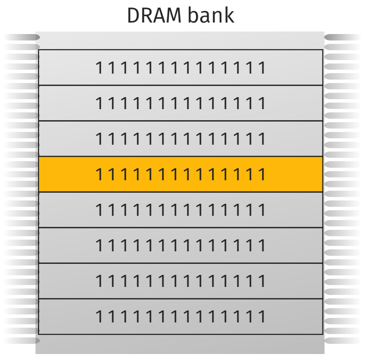

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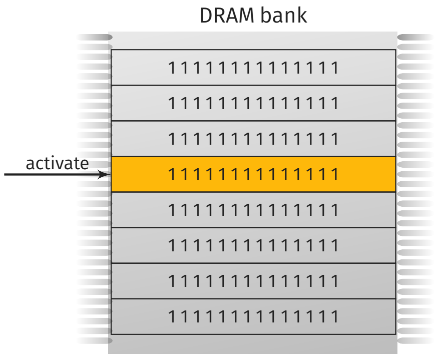

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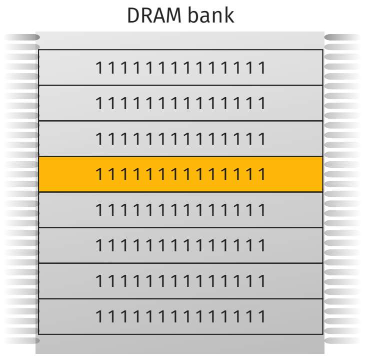

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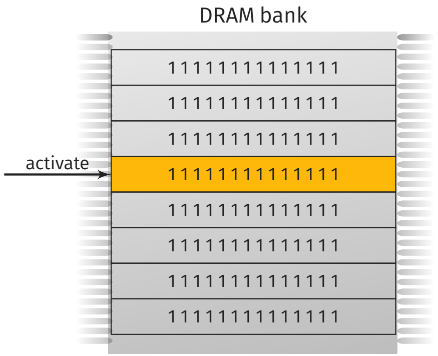

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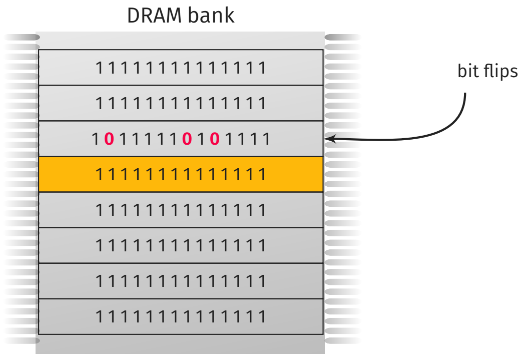
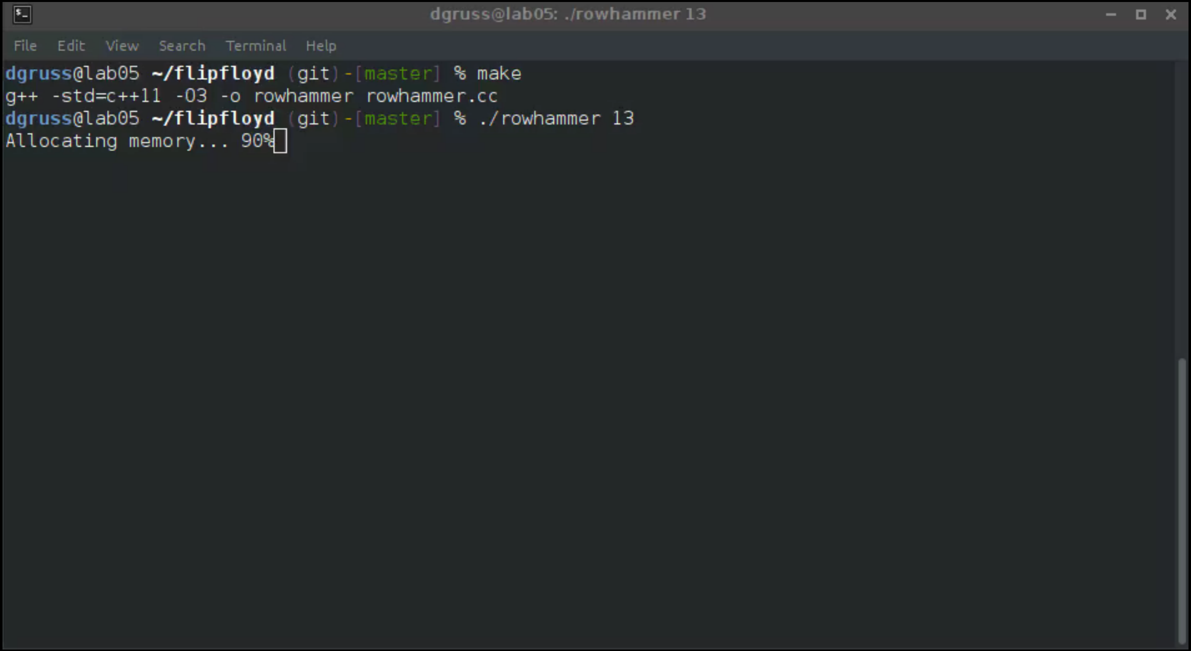
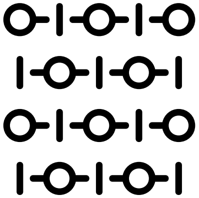



dgruss@lab05: ./rowhammer 13
File Edit View Search Terminal Help

```
dgruss@lab05 ~/flipfloyd (git)-[master] % make
g++ -std=c++11 -O3 -o rowhammer rowhammer.cc
dgruss@lab05 ~/flipfloyd (git)-[master] % ./rowhammer 13
Allocating memory... 90%
```

## Memory-Controller Policies



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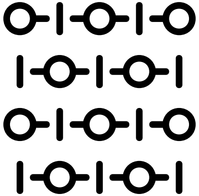

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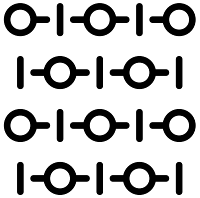

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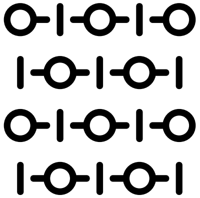

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  - Perform better on multi-core systems [Dav+11]

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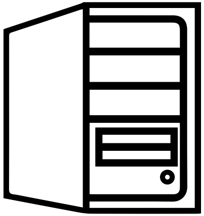
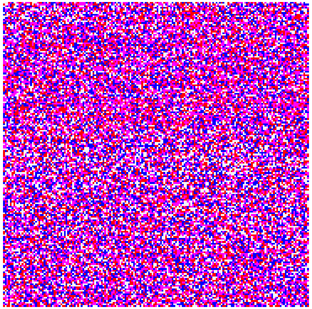


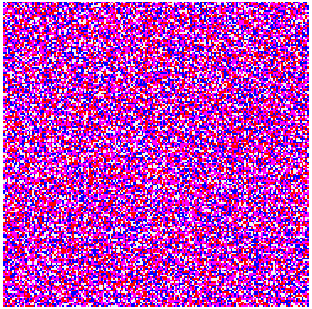
- Policies that preemptively close rows, would allow one-location hammering
- We observed close-page policies on desktop computers
- Mobile devices (e.g., laptops) seem to use mostly open-page policies

## How well does it work?


**Double-sided**

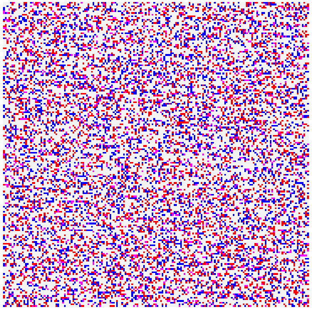
77.0 % bit offsets

51.7 % 0⟶1 bit flips


**Single-sided**

78.5 % bit offsets

54.1 % 0⟶1 bit flips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## What if we cannot target kernel pages?

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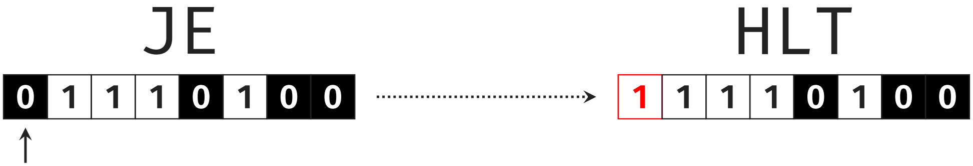
- Target `sudo` (easy to exploit)

## Opcode Flipping - Conditional Jump



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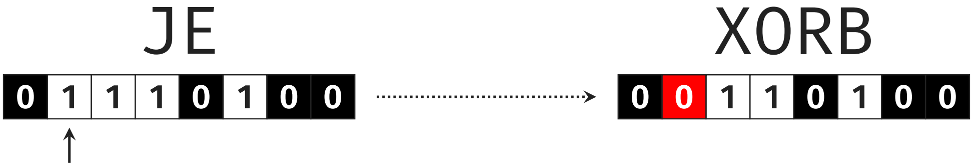

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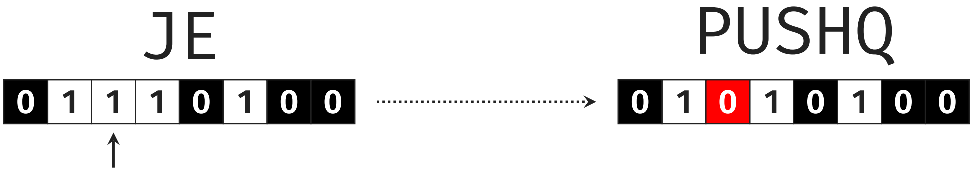

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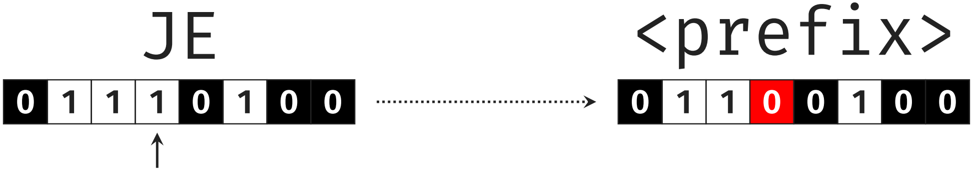

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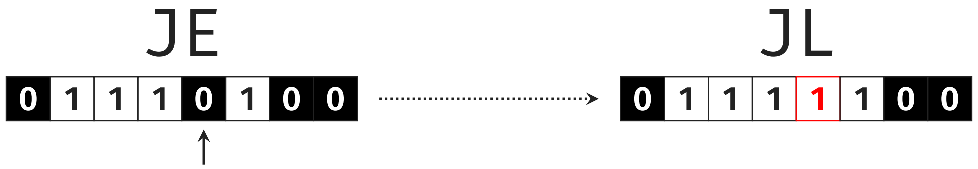

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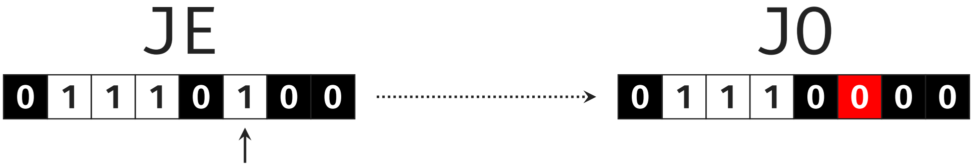

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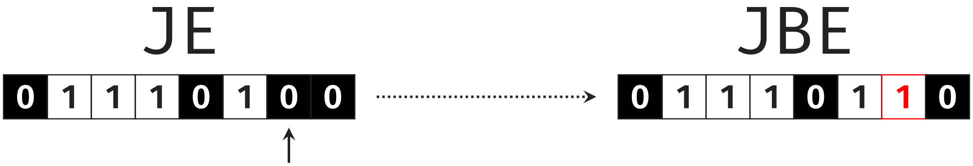

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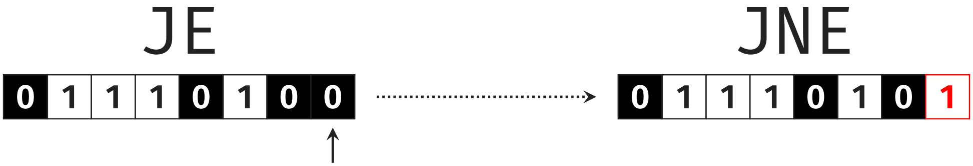

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- They all somehow skipped the password check

## How to get the target virtual page to the target physical location?

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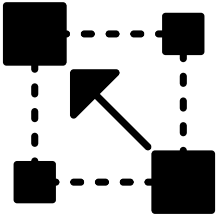
## Memory Waylaying

## Placing the binary



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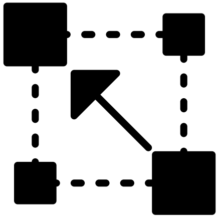

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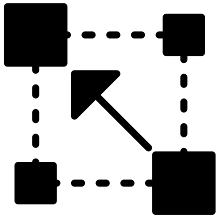
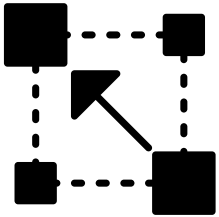


- Not as easy as with page tables
- Binary only once in memory + stays in memory (in the page cache) even after termination
- Only evicted if page cache is full

## Placing the binary



- Not as easy as with page tables
- Binary only once in memory + stays in memory (in the page cache) even after termination
- Only evicted if page cache is full
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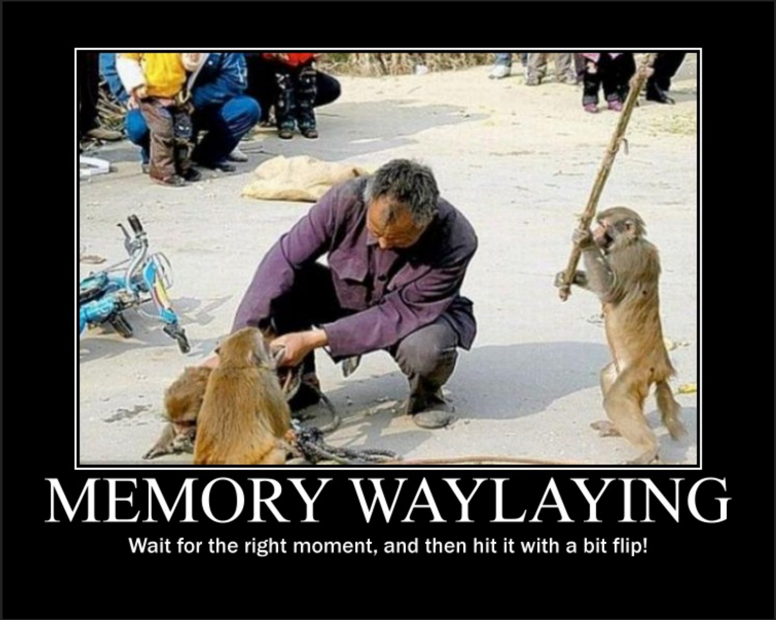
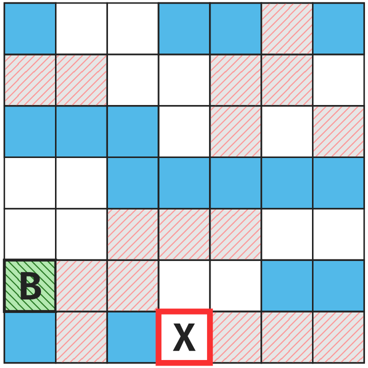
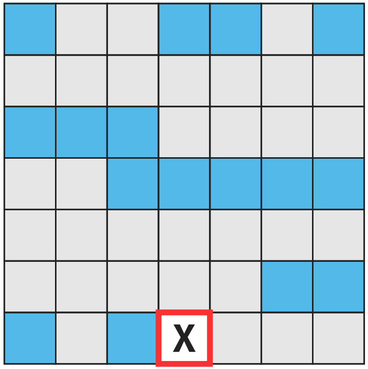

MEMORY WAYLAYING
Wait for the right moment, and then hit it with a bit flip!

Memory Waylaying

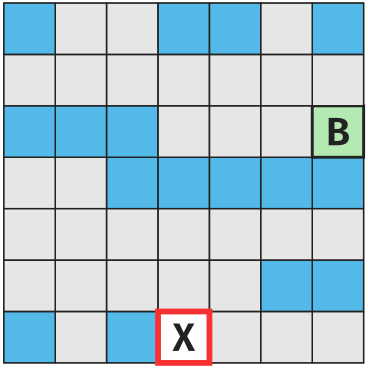
## (1) Start



## (2) Evict Page Cache

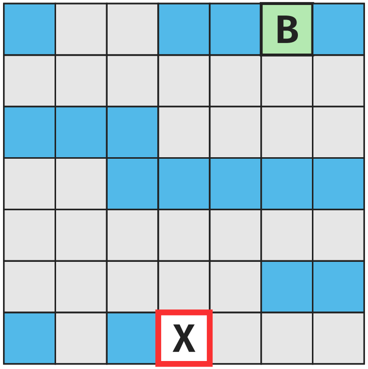


## (3) Access Binary

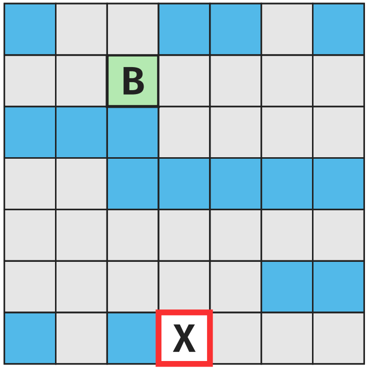


## Memory Waylaying

### (4) Evict + Access

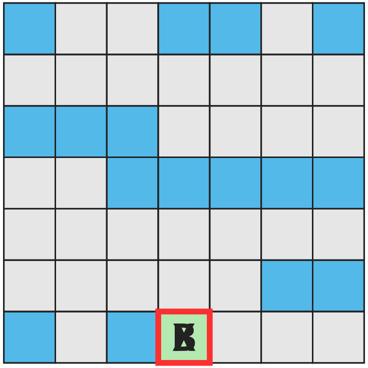


## (5) Evict + Access



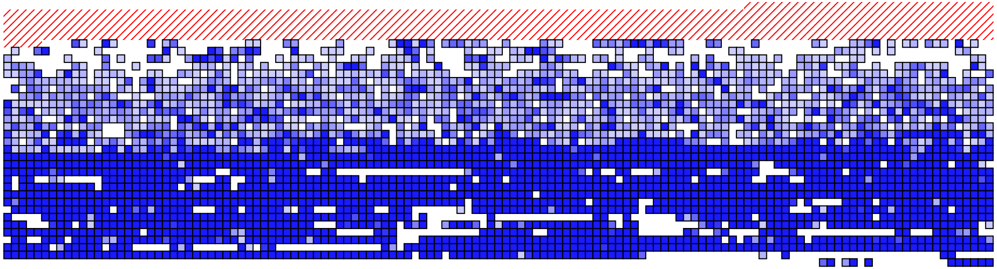
## Memory Waylaying

(6) Stop if target reached



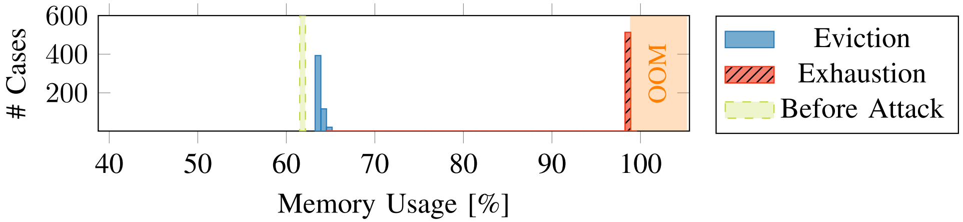
## How well does it work?

- New pages cover most of the physical memory



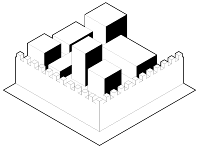
## How well does it work?

- Great advantage over memory massaging: only negligible memory footprint



## Rowhammer + SGX = Cheap Denial of Service

## Intel SGX



- Instruction-set extension
- Integrity and confidentiality of code and data in untrusted environments
- Run with user privileges and restricted, e.g., no system calls
- Run programs in enclaves using protected areas of memory

## SGX Encrypted Memory

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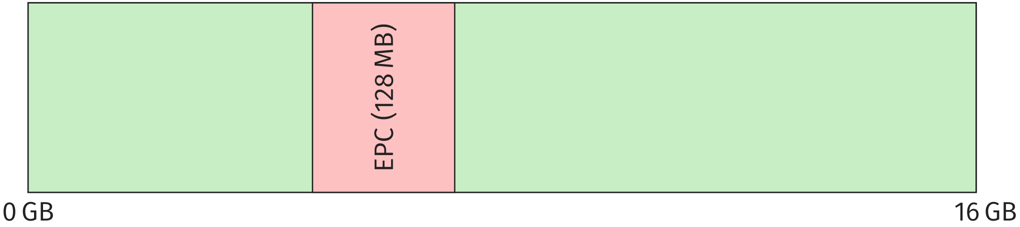
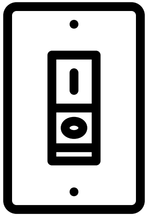


## Bit Flips in the EPC



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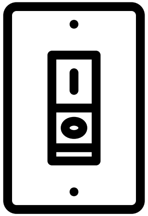

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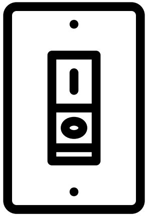

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SOUNDS UNSAFE?
IT IS UNSAFE!
imgflip.com

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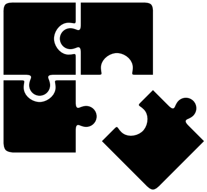
- Denial-of-Service Attacks in the Cloud [Gru+18; Jan+17]

## SGX + One-location Hammering + Opcode Flipping = Undetectable Exploit

## (Ab)using SGX Protection



- SGX protects software from malicious environments

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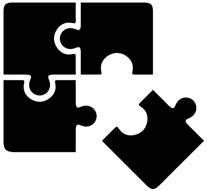

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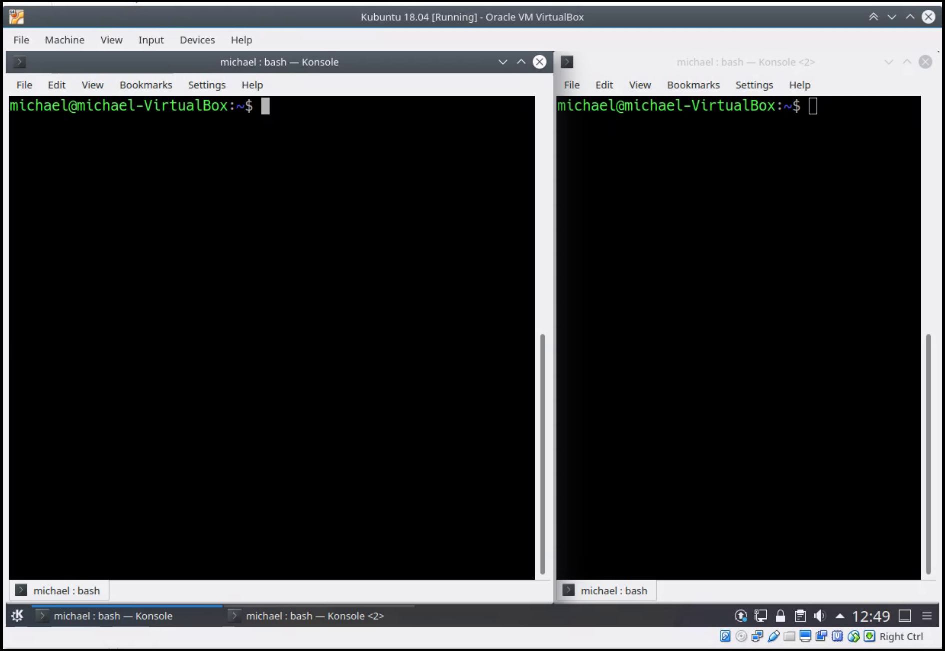
- SGX protects software from malicious environments
- Thwarts static and dynamic (= performance counters) analysis
- Hammering from SGX defeats countermeasures relying on this

STEALTH LEVEL: EXPERT


Kubuntu 18.04 [Running] - Oracle VM VirtualBox
File Machine View Input Devices Help
michael : bash — Konsole
File Edit View Bookmarks Settings Help
michael : bash — Konsole <2>
michael : bash
12:49
Right Ctrl

```
michael@michael-VirtualBox:~$
```

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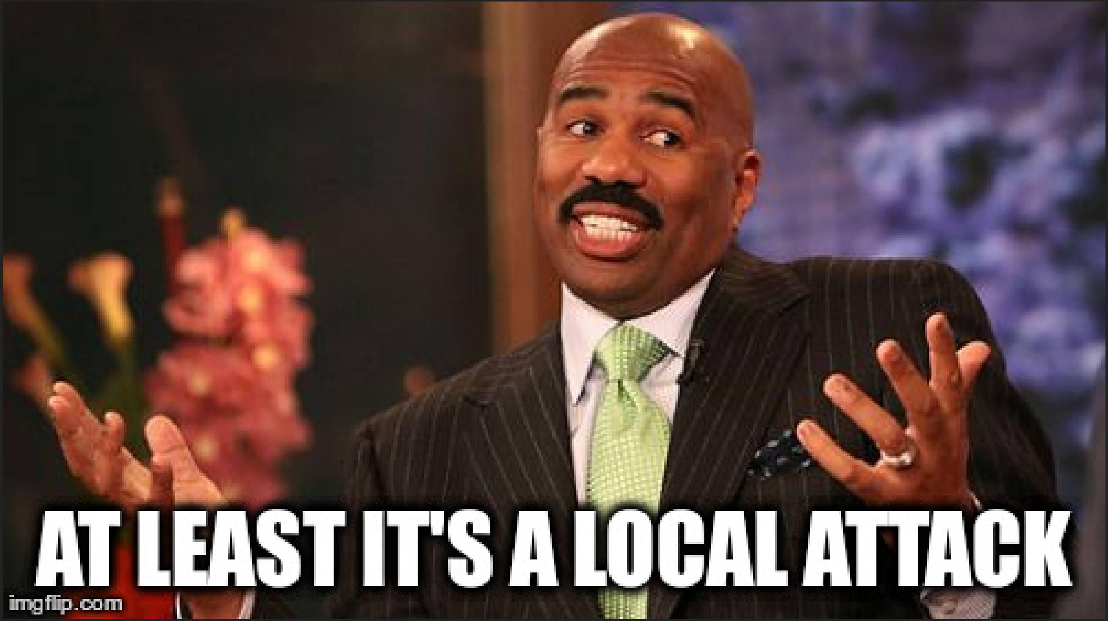
```

## Bypassing the Defenses

| Bypass \ Defense Class | Static Analysis | Performance Counters | Memory Access Pattern | Physical Proximity | Memory footprint |
|---|---|---|---|---|---|
| Intel SGX | ● | ● | ○ | ○ | ○ |
| One-location hammering | ○ | ○ | ● | ○ | ○ |
| Opcode flipping | ○ | ○ | ○ | ● | ○ |
| Memory waylaying | ○ | ○ | ○ | ○ | ● |
| **Defense class defeated** | ● | ● | ● | ● | ● |


AT LEAST IT'S A LOCAL ATTACK
imgflip.com

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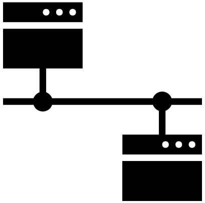
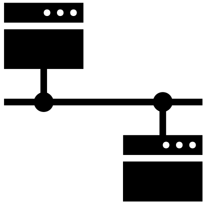


## Nethammer

Inducing bit flips:



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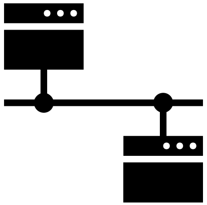

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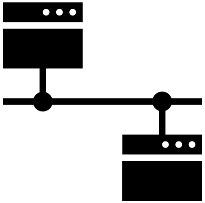

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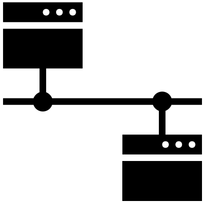

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- Network reachable code might use `clflush` or non-temporal stores (both great for hammering)

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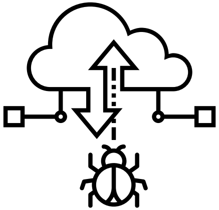

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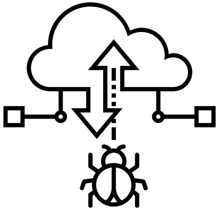

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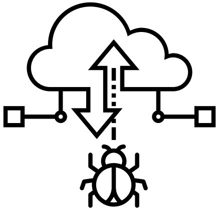

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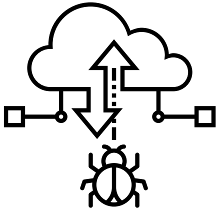

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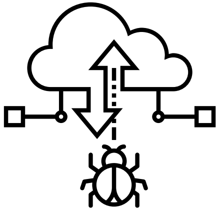

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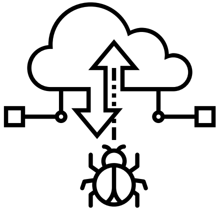

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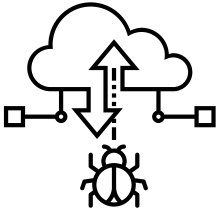

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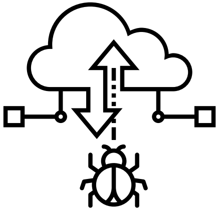

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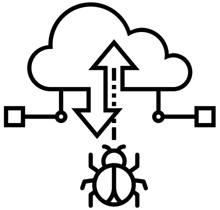

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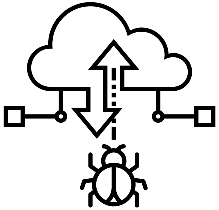

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  $\rightarrow$ Difficult to optimize with an adversary working against you

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- Moreover, new features might introduce new attack vectors (e.g., SGX)

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- More research is required to understand attacks to ultimately mitigate them

# Another Flip in the Row

Daniel Gruss, Moritz Lipp, Michael Schwarz

August 9, 2018

Graz University of Technology

## References

N. A. Anagnostopoulos, T. Arul, Y. Fan, C. Hatzfeld, A. Schaller, W. Xiong, M. Jain, M. U. Saleem, J. Lotichius, S. Gabmeyer, et al. Intrinsic Run-Time Row Hammer PUFs: Leveraging the Row Hammer Effect for Run-Time Cryptography and Improved Security. In: Cryptography 2.3 (2018), p. 13.

Z. B. Aweke, S. F. Yitbarek, R. Qiao, R. Das, M. Hicks, Y. Oren, and T. Austin. ANVIL: Software-based protection against next-generation Rowhammer attacks. In: ACM SIGPLAN Notices 51.4 (2016), pp. 743–755.

S. Bhattacharya and D. Mukhopadhyay. Curious Case of Rowhammer: Flipping Secret Exponent Bits Using Timing Analysis. In: Conference on Cryptographic Hardware and Embedded Systems (CHES). 2016.

E. Bosman, K. Razavi, H. Bos, and C. Giuffrida. Dedup Est Machina: Memory Deduplication as an Advanced Exploitation Vector. In: S&P. 2016.

F. Brasser, L. Davi, D. Gens, C. Liebchen, and A.-R. Sadeghi. CAn't Touch This: Software-only Mitigation against Rowhammer Attacks targeting Kernel Memory. In: USENIX Security Symposium. 2017.

J. Corbet. Defending against Rowhammer in the kernel. Oct. 2016. URL: `https://lwn.net/Articles/704920/`.

M. Chiappetta, E. Savas, and C. Yilmaz. Real time detection of cache-based side-channel attacks using Hardware Performance Counters. Cryptology ePrint Archive, Report 2015/1034. 2015.

Y. Cheng, Z. Zhang, and S. Nepal. Still Hammerable and Exploitable: on the Effectiveness of Software-only Physical Kernel Isolation. In: arXiv:1802.07060 (2018).

H. David, C. Fallin, E. Gorbatov, U. R. Hanebutte, and O. Mutlu. Memory power management via dynamic voltage/frequency scaling. In: ACM International Conference on Autonomic Computing. 2011.

P. Frigo, C. Giuffrida, H. Bos, and K. Razavi. Grand Pwning Unit: Accelerating Microarchitectural Attacks with the GPU. In: IEEE S&P. 2018.

D. Gruss, C. Maurice, and S. Mangard. Rowhammer.js: A Remote Software-Induced Fault Attack in JavaScript. In: DIMVA. 2016.

D. Gruss, C. Maurice, K. Wagner, and S. Mangard. Flush+Flush: A Fast and Stealthy Cache Attack. In: DIMVA. 2016.

D. Gruss, M. Lipp, M. Schwarz, D. Genkin, J. Juffinger, S. O'Connell, W. Schoechl, and Y. Yarom. Another Flip in the Wall of Rowhammer Defenses. In: S&P. 2018.

N. Herath and A. Fogh. These are Not Your Grand Daddys CPU Performance Counters – CPU Hardware Performance Counters for Security. In: Black Hat Briefings. Aug. 2015. URL: https://www.blackhat.com/docs/us-15/materials/us-15-Herath-These-Are-Not-Your-Grand-Daddys-CPU-Performance-Counters-CPU-Hardware-Performance-Counters-For-Security.pdf.

G. Irazoqui, T. Eisenbarth, and B. Sunar. MASCAT: Stopping Microarchitectural Attacks Before Execution. Cryptology ePrint Archive, Report 2016/1196. 2017.

Y. Jang, J. Lee, S. Lee, and T. Kim. SGX-Bomb: Locking Down the Processor via Rowhammer Attack. In: SysTEX. 2017.

Y. Kim, R. Daly, J. Kim, C. Fallin, J. H. Lee, D. Lee, C. Wilkerson, K. Lai, and O. Mutlu. Flipping bits in memory without accessing them: An experimental study of DRAM disturbance errors. In: ISCA'14. 2014.

M. Lanteigne. How Rowhammer Could Be Used to Exploit Weaknesses in Computer Hardware. Mar. 2016. URL: http://www.thirdio.com/rowhammer.pdf.

M. Lipp, M. T. Aga, M. Schwarz, D. Gruss, C. Maurice, L. Raab, and L. Lamster. Nethammer: Inducing Rowhammer Faults through Network Requests. In: arXiv:1711.08002 (2017).

M. Payer. HexPADS: a platform to detect "stealth" attacks. In: ESSoS'16. 2016.

P. Pessl, D. Gruss, C. Maurice, M. Schwarz, and S. Mangard. DRAMA: Exploiting DRAM Addressing for Cross-CPU Attacks. In: USENIX Security Symposium. 2016.

D. Poddebniak, J. Somorovsky, S. Schinzel, M. Lochter, and P. Rösler. Attacking deterministic signature schemes using fault attacks. In: EuroS&P. 2018.

R. Qiao and M. Seaborn. A New Approach for Rowhammer Attacks. In: International Symposium on Hardware Oriented Security and Trust. 2016.

K. Razavi, B. Gras, E. Bosman, B. Preneel, C. Giuffrida, and H. Bos. Flip Feng Shui: Hammering a Needle in the Software Stack. In: USENIX Security Symposium. 2016.

M. Seaborn and T. Dullien. Exploiting the DRAM rowhammer bug to gain kernel privileges. In: Black Hat Briefings. 2015.

A. Tatar, R. Krishnan, E. Athanasopoulos, C. Giuffrida, H. Bos, and K. Razavi. Throwhammer: Rowhammer Attacks over the Network and Defenses. In: USENIX ATC. 2018.

V. van der Veen, Y. Fratantonio, M. Lindorfer, D. Gruss, C. Maurice, G. Vigna, H. Bos, K. Razavi, and C. Giuffrida. Drammer: Deterministic Rowhammer Attacks on Mobile Platforms. In: CCS'16. 2016.

V. van der Veen, M. Lindorfer, Y. Fratantonio, H. P. Pillai, G. Vigna, C. Kruegel, H. Bos, and K. Razavi. GuardION: Practical Mitigation of DMA-Based Rowhammer Attacks on ARM. In: DIMVA. 2018.

Y. Xiao, X. Zhang, Y. Zhang, and R. Teodorescu. One Bit Flips, One Cloud Flops: Cross-VM Row Hammer Attacks and Privilege Escalation. In: USENIX Security Symposium. 2016.

## Runtime of the attack

| Method | Bit flips | Templating | Waylaying | Total |
|---:|---:|---:|---:|---:|
| Double-sided, waylaying | 91 | 26.1 h | 69.4 h | 95.5 h |
| Single-sided, waylaying | 87 | 27.5 h | 70.6 h | 98.1 h |
| One-location, waylaying | 50 | 47.3 h | 90.5 h | 137.8 h |
| Double-sided, chasing | 1 | 0.7 h | 43.7 h | 44.4 h |
| Single-sided, chasing | 1 | 0.7 h | 43.7 h | 44.4 h |
| One-location, chasing | 1 | 1.3 h | 44.0 h | 45.4 h |