DRAMA: How your DRAM becomes a security problem

Michael Schwarz and Anders Fogh

November 4, 2016

About this presentation

This talk is about how DRAM leaks information across security boundries

- Not about software bugs
- It is about hardware design becomes an attack vector
- Focus on Intel x86-64 - but problem is DRAM - thus applies to other architectures as well

Take aways

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- DRAM design is security relevant
- DRAM leaks information

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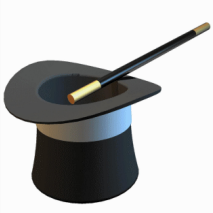
Exploit this to:

- Covertly extract information cross VM, cross CPU
- Spy on other software
- Enable efficient and targeted row hammer attacks

Introduction

Demo



DEMO

What you just saw

- 0 software bugs
- Covert communication in and out of VM
- Covert communication in and out of JS sandbox
- This isn’t magic..

Whoami

- Michael Schwarz
- PhD Student, Graz University of Technology
- Likes to break stuff
- Twitter: `@misc0110`
- Email: `michael.schwarz@iaik.tugraz.at`

And the team

The research team

- Peter Pessl
- Daniel Gruss
- Clémentine Maurice
- Stefan Mangard

from Graz University of Technology

Whoami

- Anders Fogh
- Principal Security Researcher, GDATA Advanced Analytics
- Playing with malware since 1992
- Twitter: `@anders_fogh`
- Email: `anders.fogh@gdata-adan.de`

From code to capacitor

From code to capacitor

MOV RAX, [0x4141414141]

TO

Page tables

Virtual and physical addressing

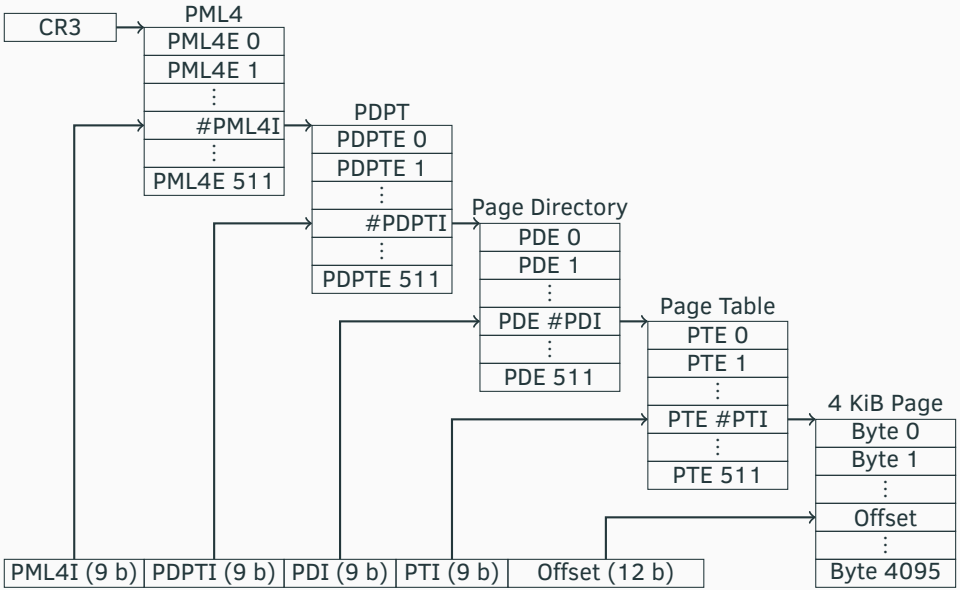
- 0x41414141 is a virtual address of the current process
- The CPU need a physical address to talk to DRAM
- Thus translation is needed

Why translation

Why address translation: Run multiple processes securely on a single CPU

- Let applications run in their own virtual address space
- Create exchangeable map from “virtual memory” to “physical memory”
- Privileges are checked on memory accesses
- Managed by the operating system kernel and hypervisor

Address translation on x86-64



Virtual and physical addressing

Summary:

- The most significant bits of the virtual address determines the page
- A page is almost always $4\,\mathrm{kB}$ large
- The least significant bits (almost always 12 bits) is an offset into the page
- Only the page is translated and security checked

Data caches

Road block: Data Caches

Memory (DRAM) is slow compared to the CPU

- buffer frequently used memory for the CPU
- every memory reference goes through the cache
- transparent to OS and programs

= Problem: We want to speak to DRAM, not a cache

Bypass cache road block

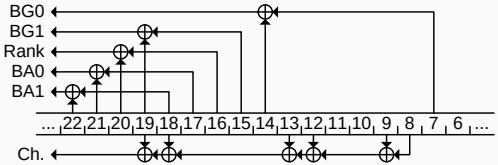
We must remove our address from the cache to talk to DRAM

- Native code: CLFLUSH instruction
- Javascript: Evict Gruss et al. 2016

The memory controller

How does physical addresses map to memory

Memory controller in the processor has a mapping function



Based on physical addresses

How is DRAM organized?

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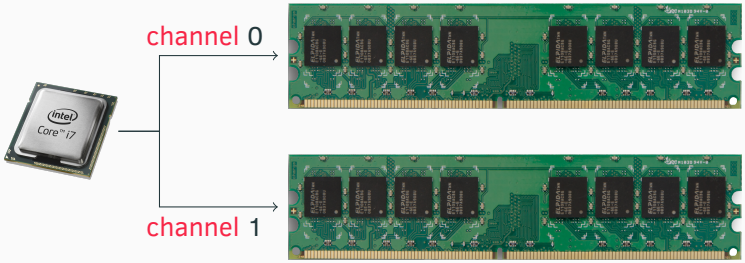

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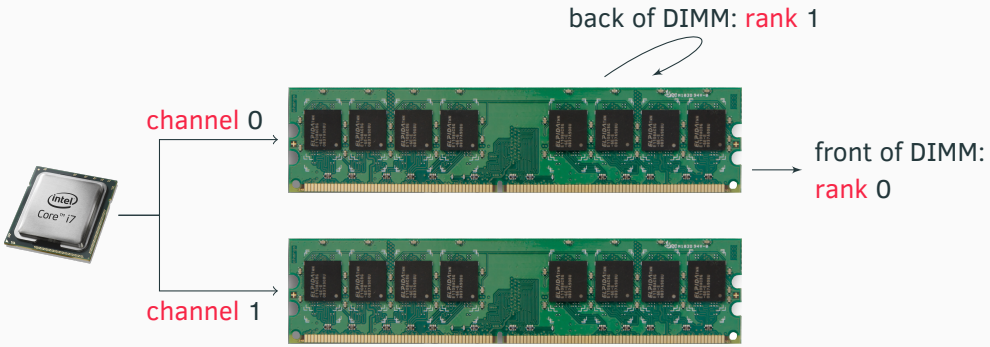

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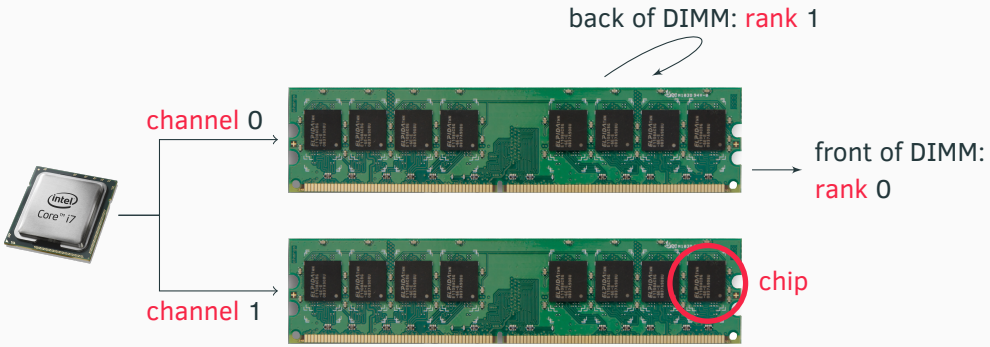


DRAM organization

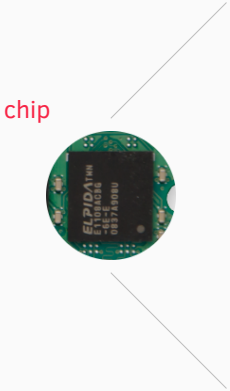
chip

bank 0

row 0
row 1
row 2
...
row 32767

row buffer

DRAM organization



First hint of trouble

- A row is 64k Cells: $8\,\mathrm{kB}$
- Security was checked for $4\,\mathrm{kB}$ blocks

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= security domains may share rows

Reading from DRAM

The Row buffer

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- Capacitors in cells discharge when you “read the bits”
- Buffer the bits when reading them from the cells
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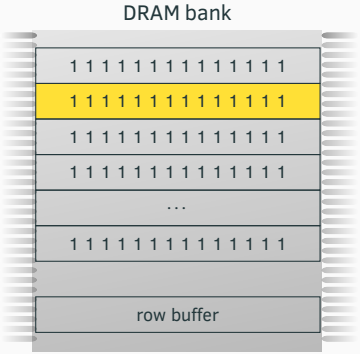

CPU reads row 1,
row buffer empty!

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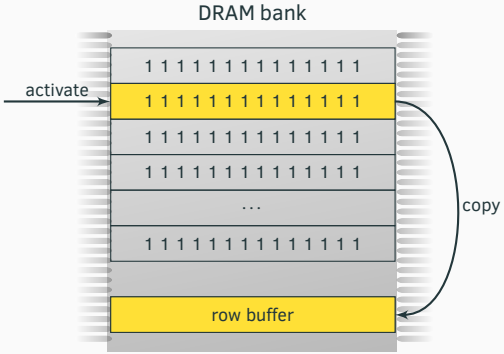

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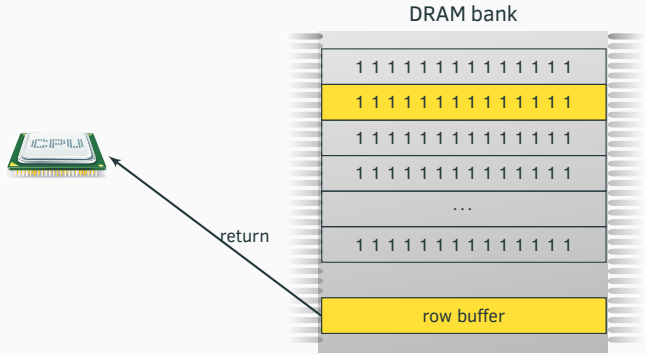

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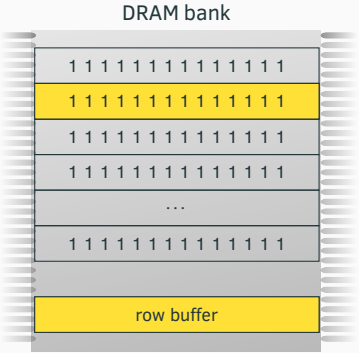
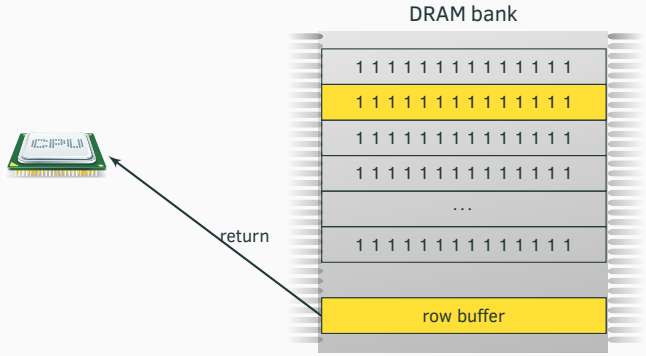


CPU reads row 1,
row buffer now full!

How reading from DRAM works



Less work!
Is it faster?

We can measure a difference

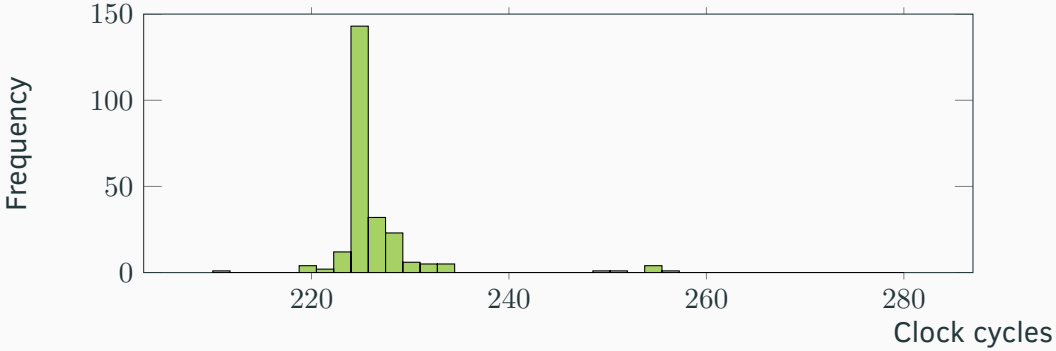


Figure 1: Row hits

We can measure a difference

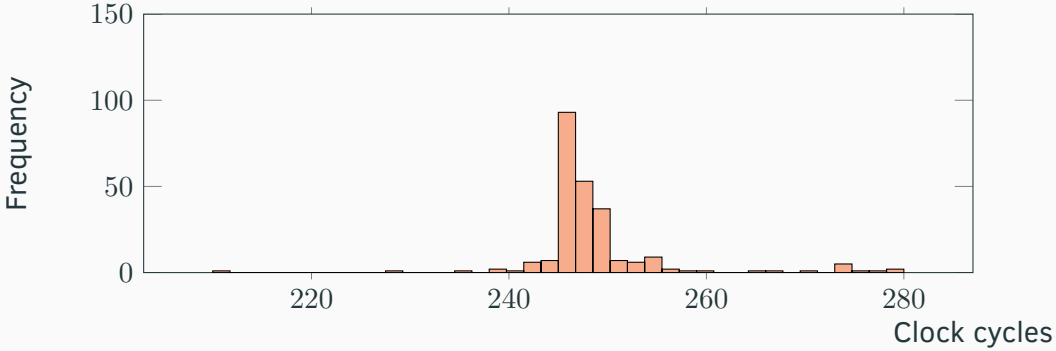
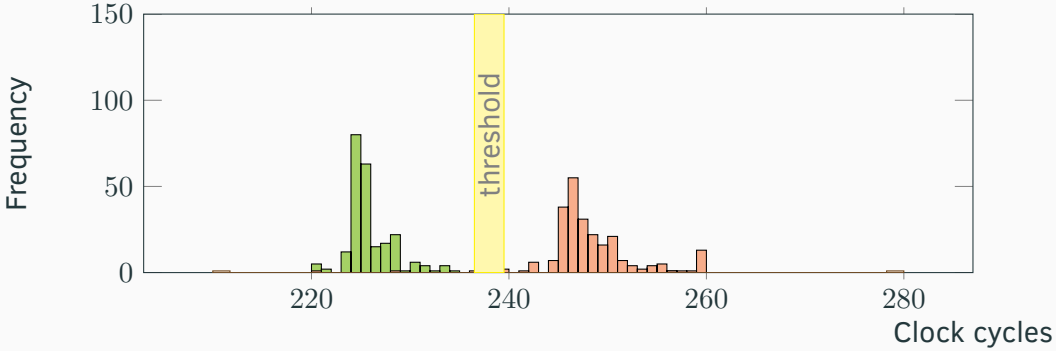


Figure 2: Row conflicts

We can measure a difference



Difference between row hits ($\approx$ 225 cycles) and row conflicts ($\approx$ 247 cycles) on an Intel Core i7 Ivy Bridge machine.

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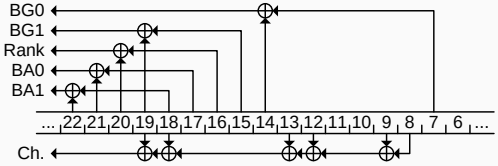
= DRAM leaks information

First attack: Reversing the CPU

Remember this?

Memory controller in the processor has a mapping function



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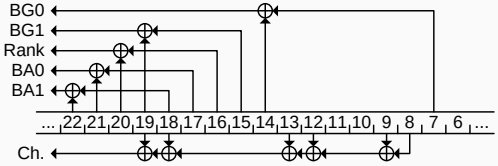


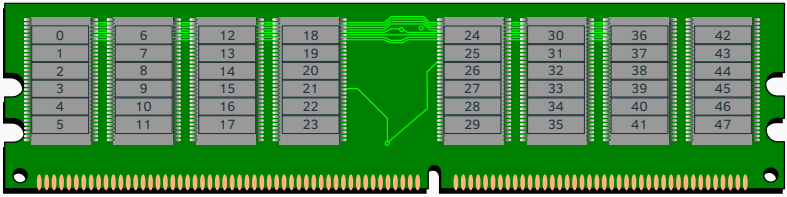
- Based on physical addresses
- Problem: this function is undocumented

Reversing the mapping function

Reverse engineer the mapping function

- You can reverse engineer the mapping of your processor using row hits and misses

Reversing the mapping function - Approach



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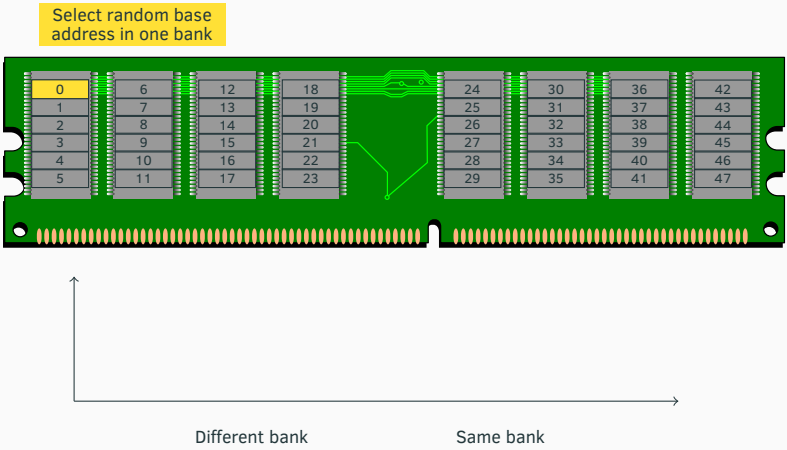

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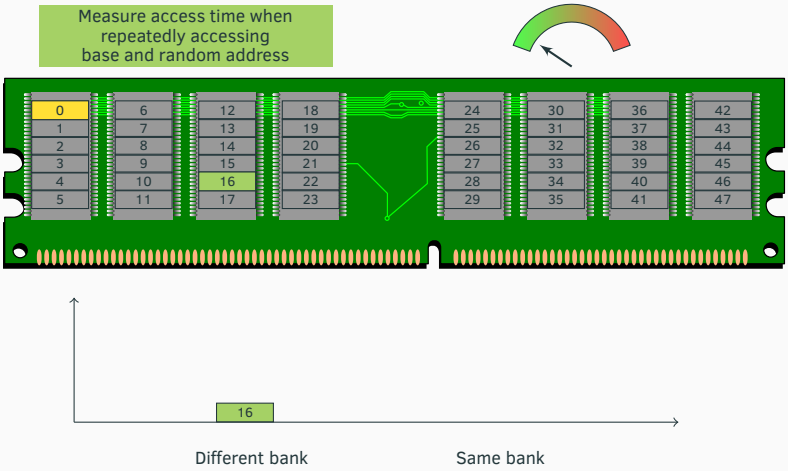

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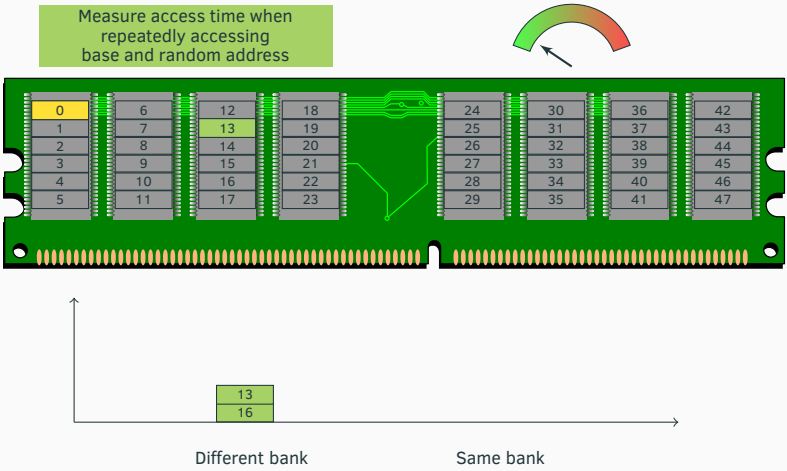

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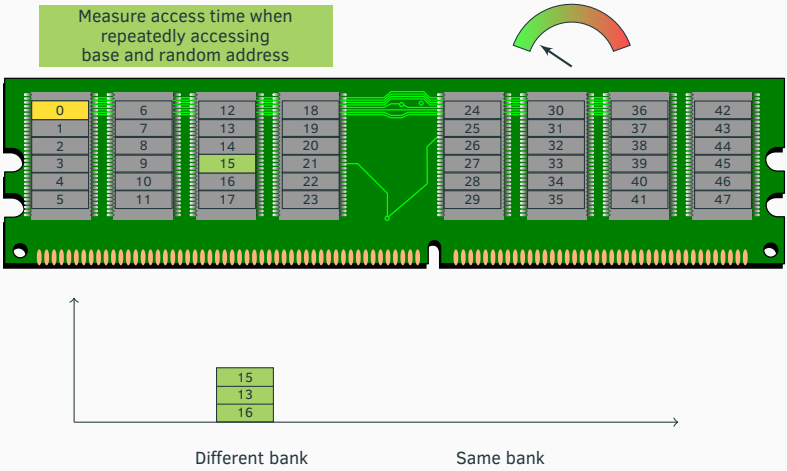

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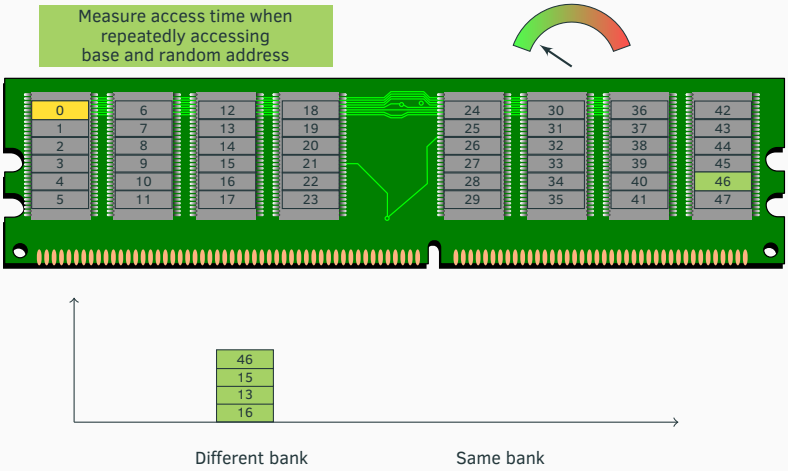

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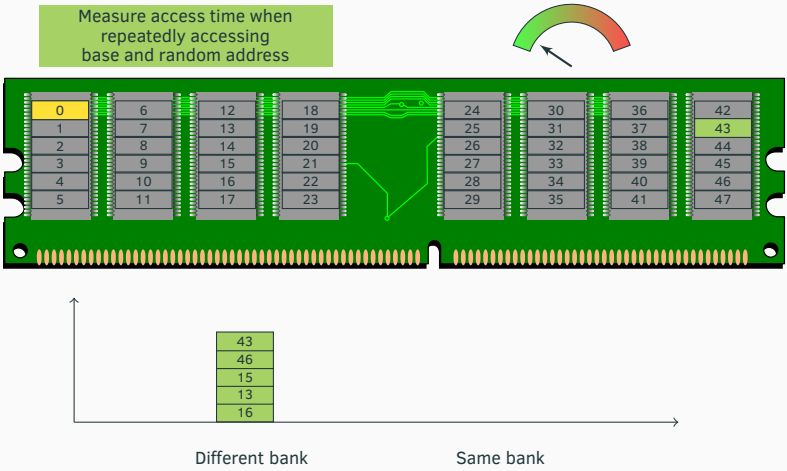

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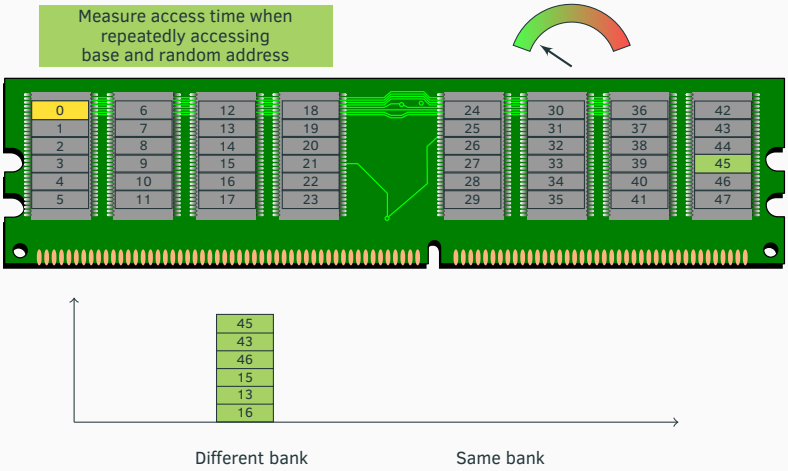

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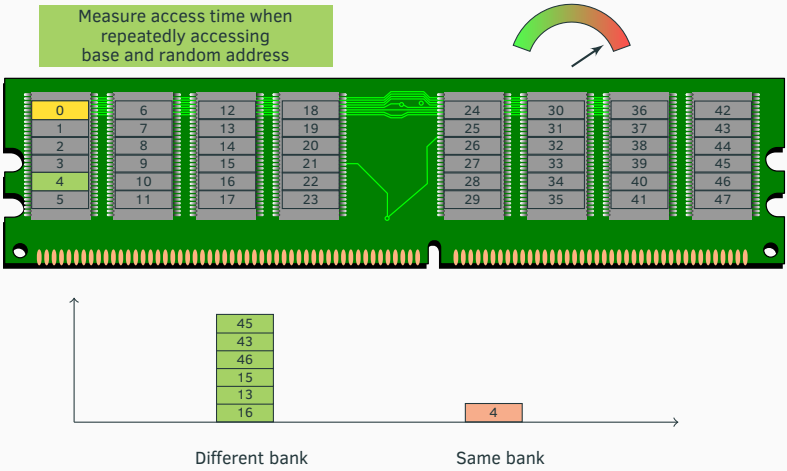

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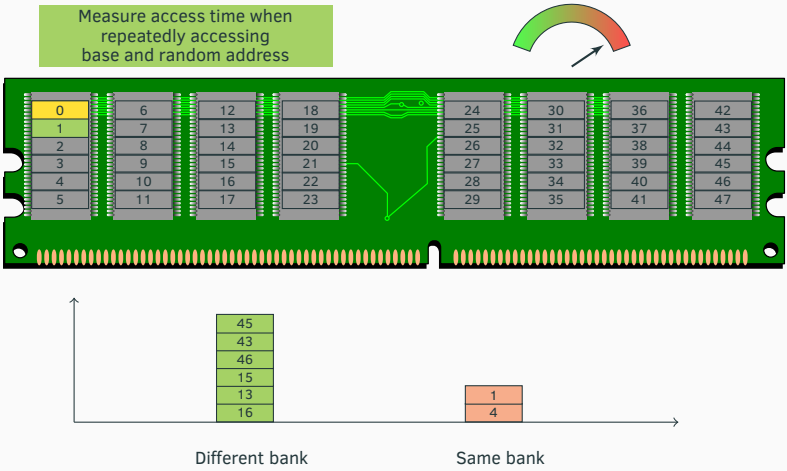

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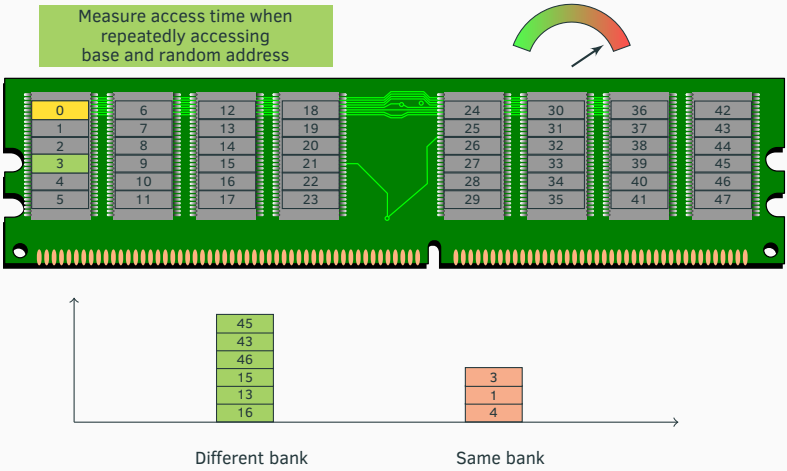
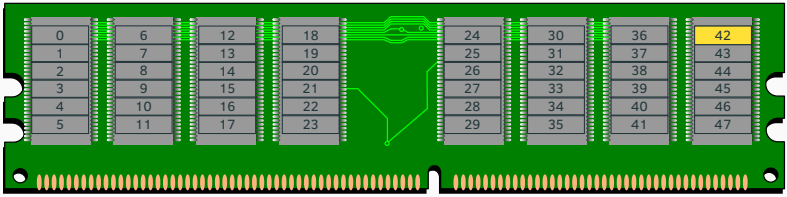


Reversing the mapping function - Approach

Select random base address in one bank



Different bank

Same bank

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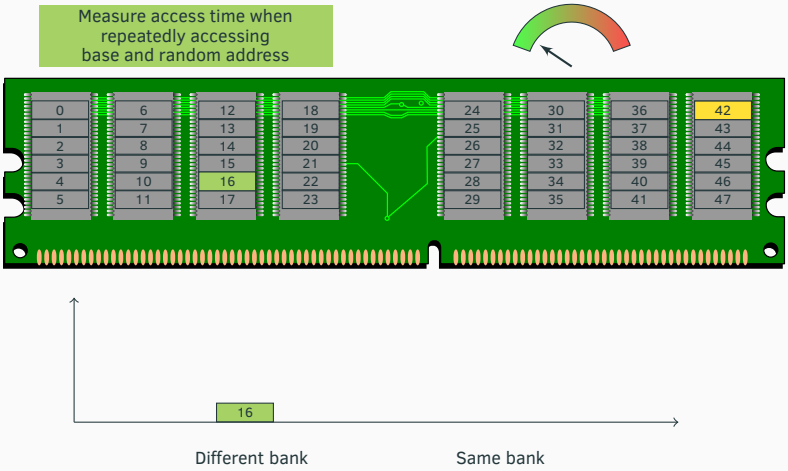

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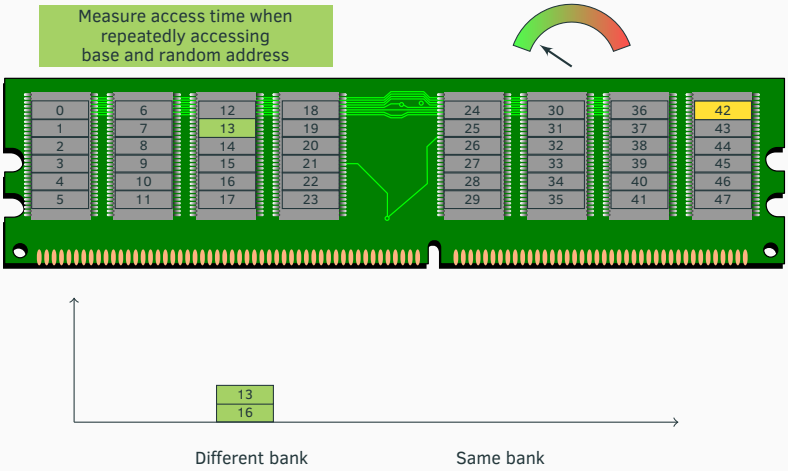

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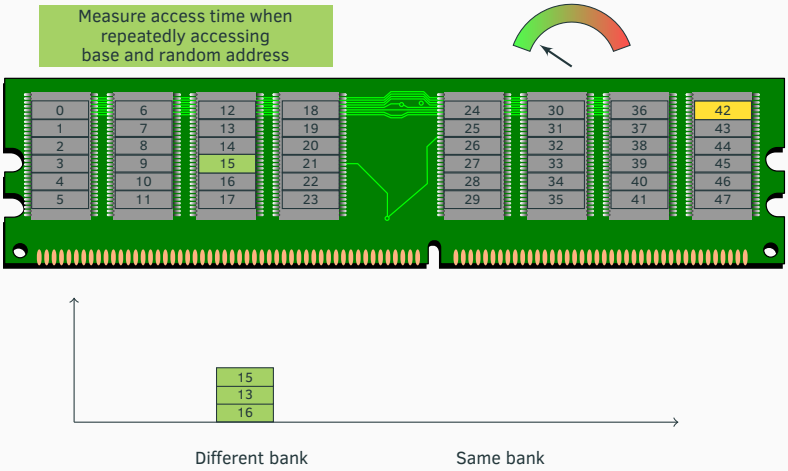

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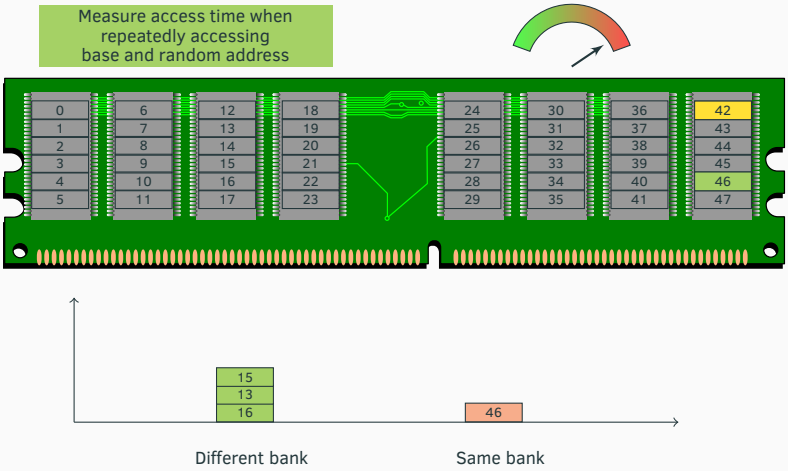

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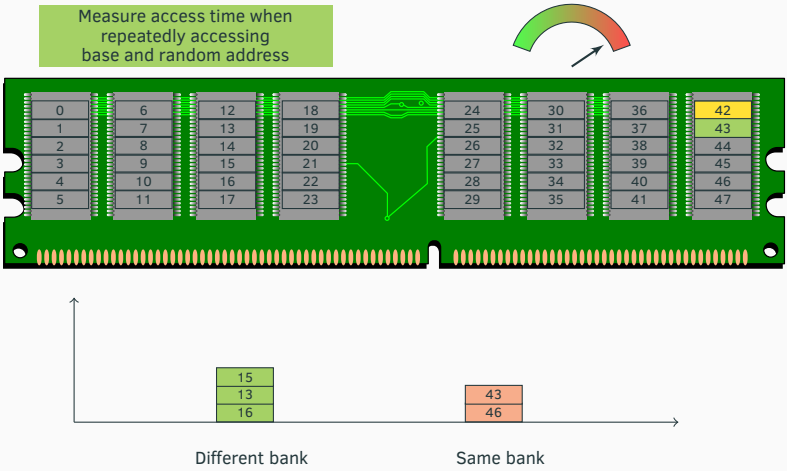

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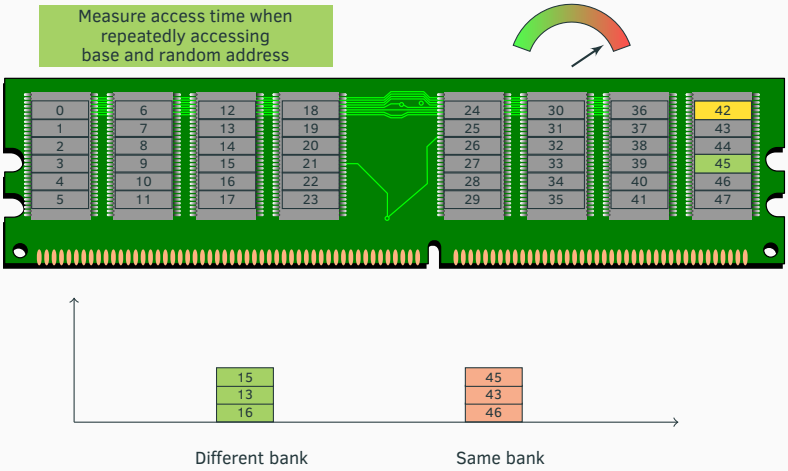

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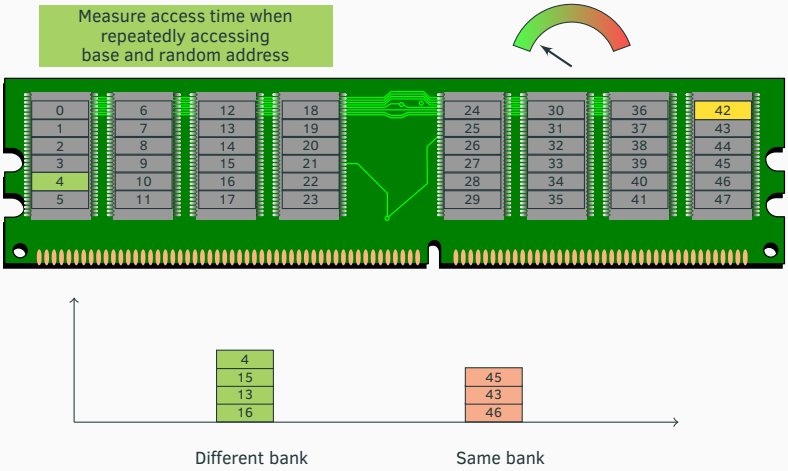

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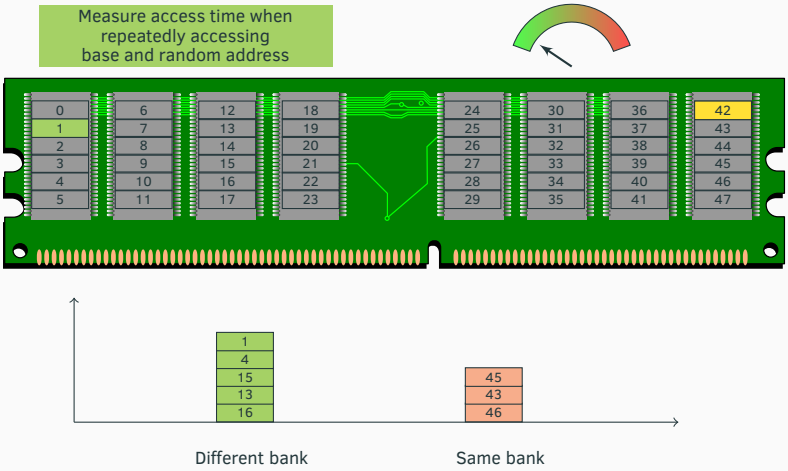

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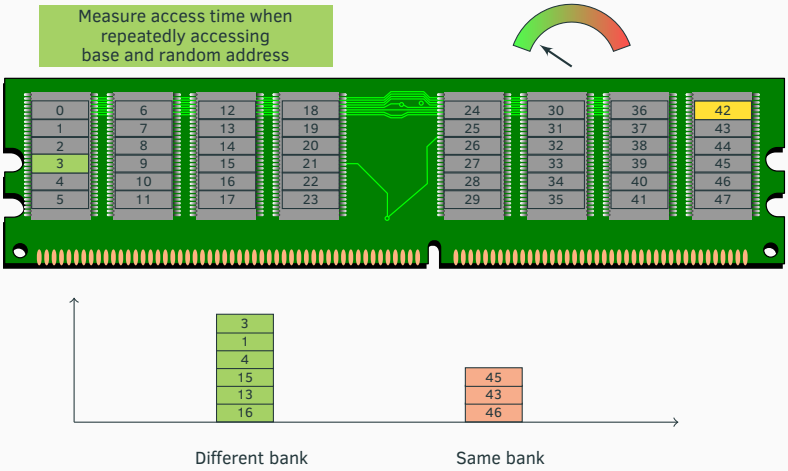

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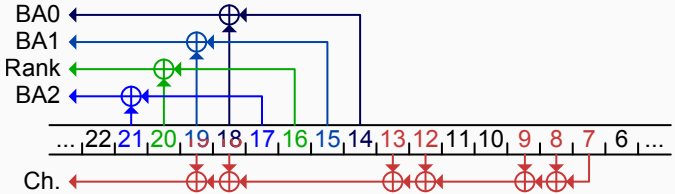
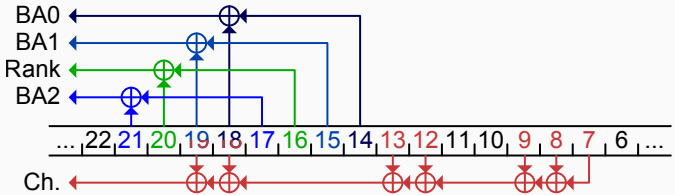
- The alternative: generate every possible XOR function and check if it yields the same result for all addresses in the set
- This is still very fast (in the order of seconds)

Results



- We developed a toolkit that reverse engineers the mapping fully automatically

Results



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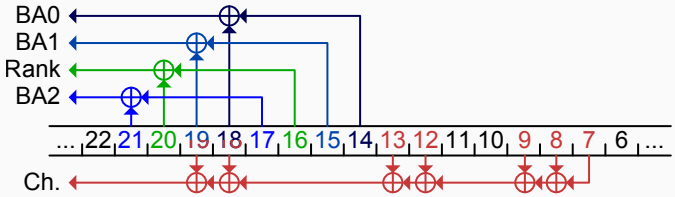

- We developed a toolkit that reverse engineers the mapping fully automatically
- Takes between seconds and minutes
- You can download it here: https://github.com/IAIK/drama

What next?

- We know which address maps to which part of the DRAM

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What next?

- We know which address maps to which part of the DRAM
- We can do that fully automatic on any new system
- Once we have the function, we can exploit that knowledge


Stay Tuned
FOR
something
Awesome

Spying through the DRAM

Imagine this code

```
WCHAR WideCharFromScanCode(unsigned short scancode)
{
    if (IsUpperCase(scancode))
    {
        return HandleUpperCase(scancode);
    }
    else
    {
        return HandleLowerCase(scancode);
    }
}
```

Spying

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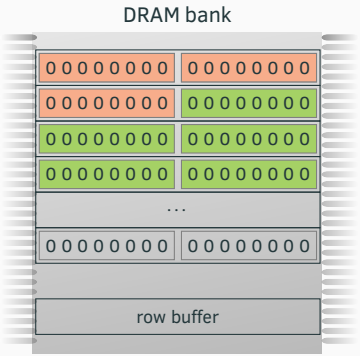
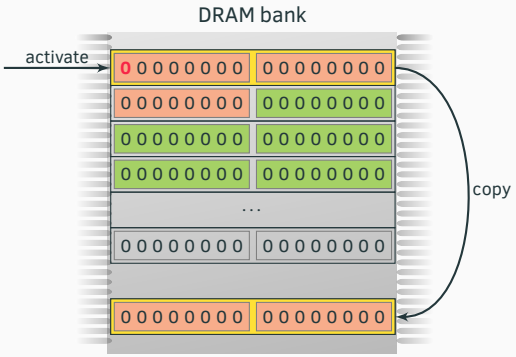
- We can use row hits to get useful information
- Advantage over cache attacks: it works across CPUs

Attack Primitive: Row hit



Spy activates row 0, get copied to row buffer

Attack Primitive: Row hit



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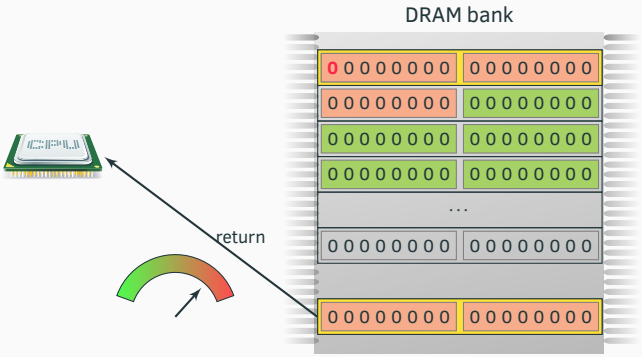

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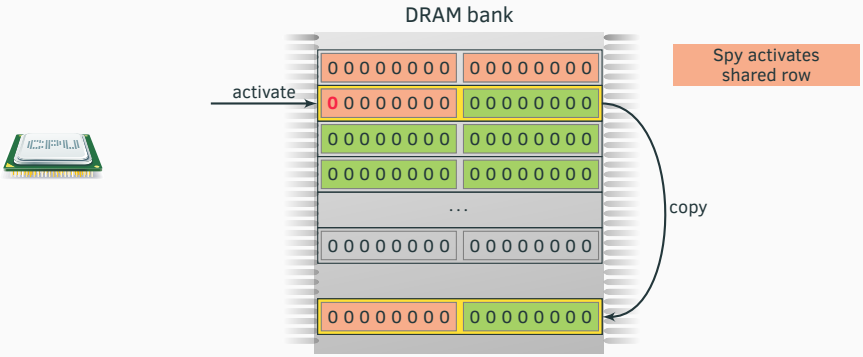

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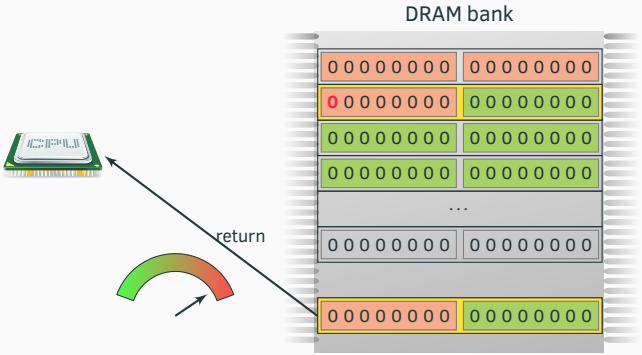

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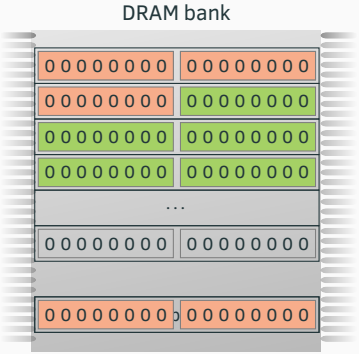

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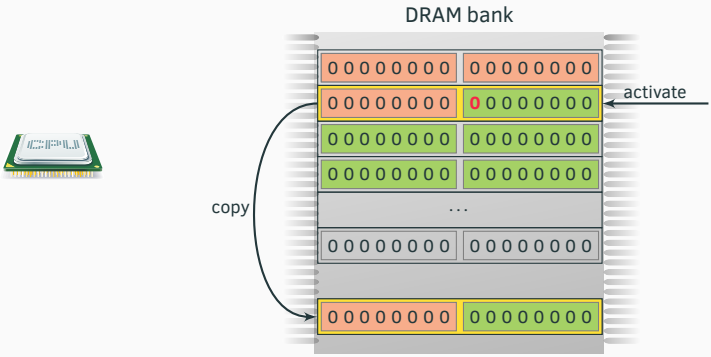

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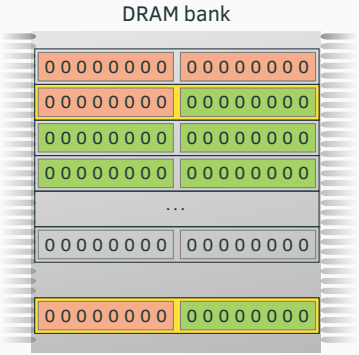
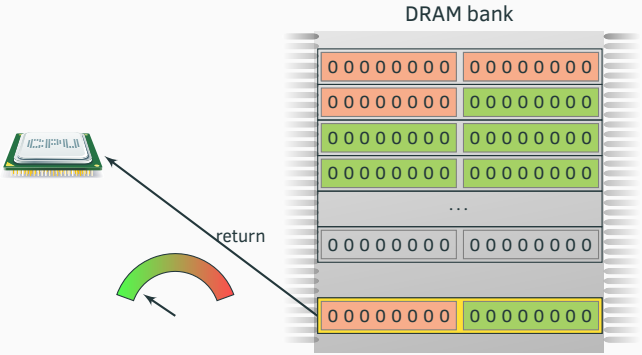


...before the spy activates it

Attack Primitive: Row hit



Row hit, faster

Two related questions

- What is the chance we can share a row with important victim data?

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- What is the chance we can share a row with important victim data?
- What kind of spatial accuracy will we get?

Row hits

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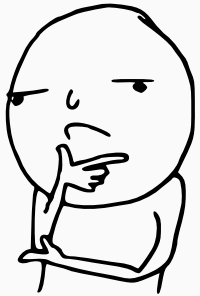

Accuracy

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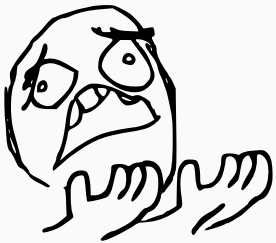
Accuracy



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- Why?

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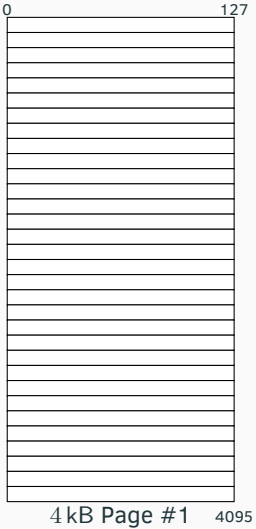
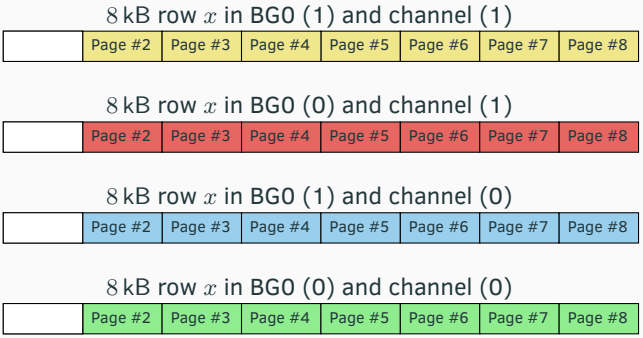
- One physical page is distributed over 4 rows

Accuracy


0
127
4 kB Page #1
4095


8 kB row x in BG0 (1) and channel (1)
Page #2
Page #3
Page #4
Page #5
Page #6
Page #7
Page #8
8 kB row x in BG0 (0) and channel (1)
Page #2
Page #3
Page #4
Page #5
Page #6
Page #7
Page #8
8 kB row x in BG0 (1) and channel (0)
Page #2
Page #3
Page #4
Page #5
Page #6
Page #7
Page #8
8 kB row x in BG0 (0) and channel (0)
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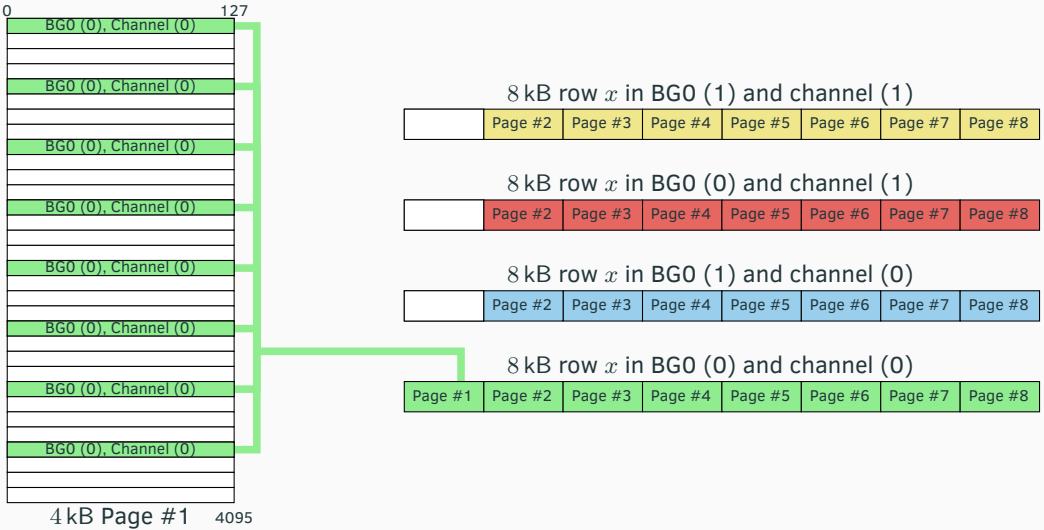
Accuracy


0
127
BG0 (0), Channel (0)
BG0 (0), Channel (0)
BG0 (0), Channel (0)
BG0 (0), Channel (0)
BG0 (0), Channel (0)
BG0 (0), Channel (0)
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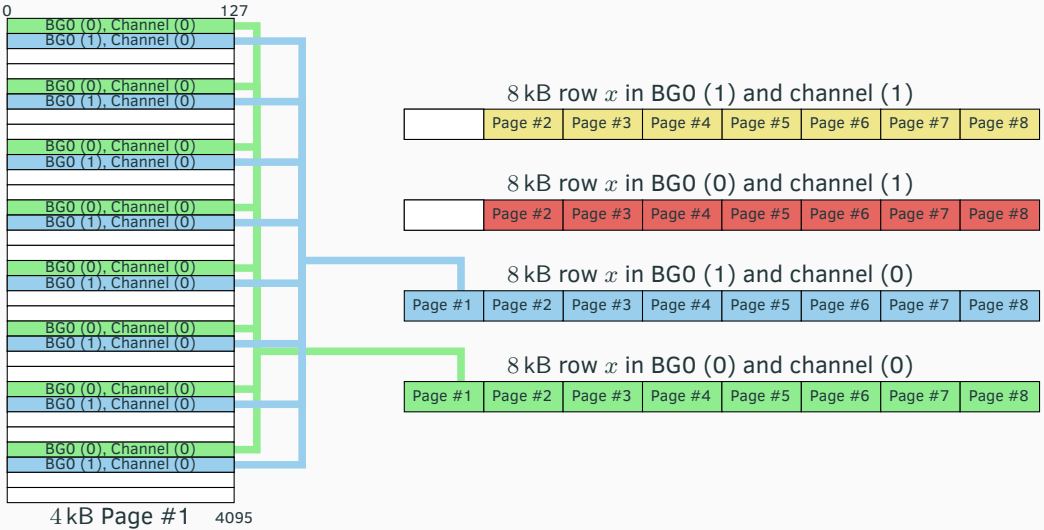
0
127
BG0 (0), Channel (0)
BG0 (1), Channel (0)
4 kB Page #1
4095
8 kB row x in BG0 (1) and channel (1)
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Page #1
8 kB row x in BG0 (0) and channel (0)

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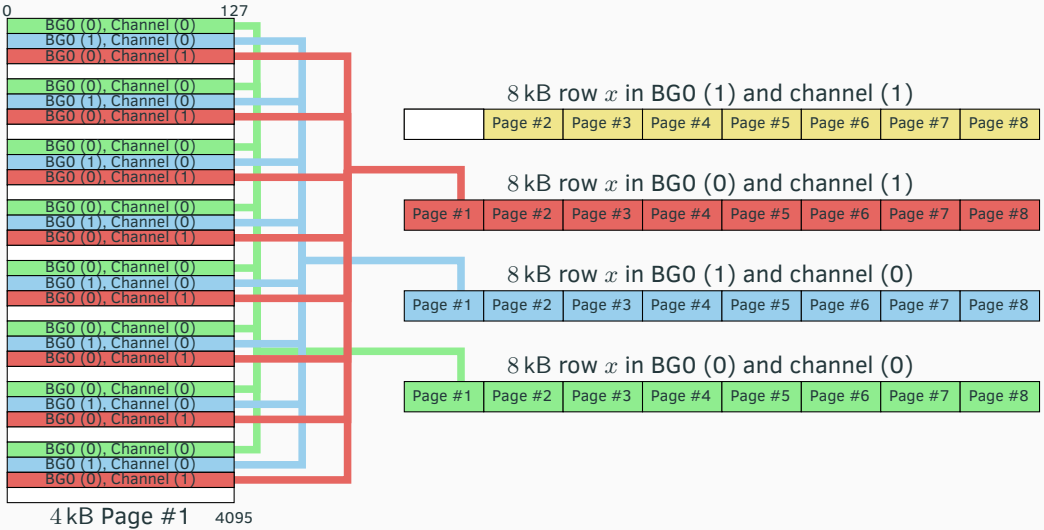
0
127
BG0 (0), Channel (0)
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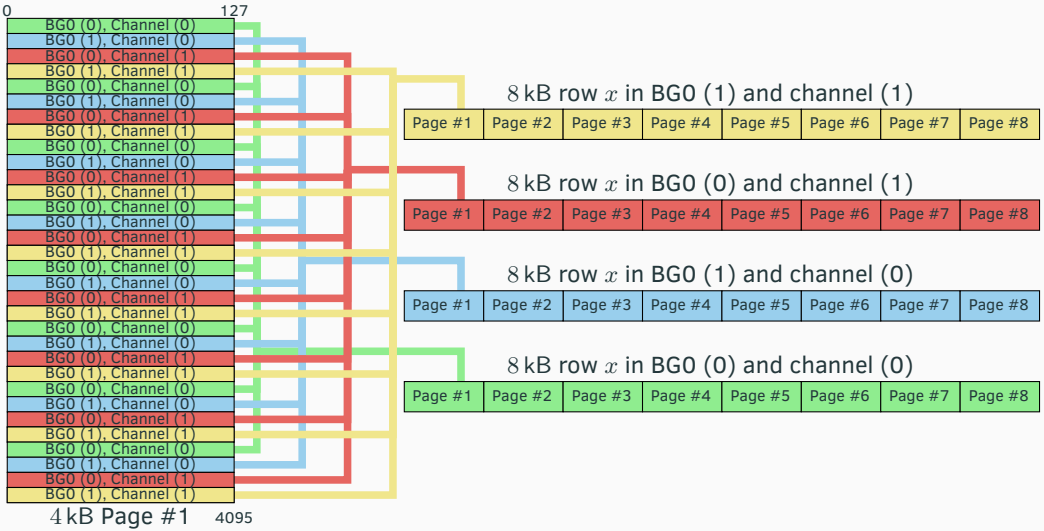
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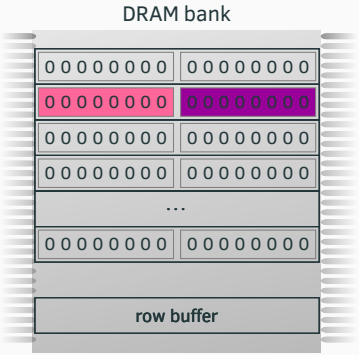
Results

Row sharing

Sandy Bridge /w 1 DIMM

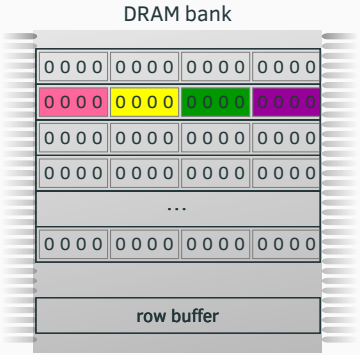


2 pages per row

Results

Row sharing

Ivy Bridge /w 2 DIMM

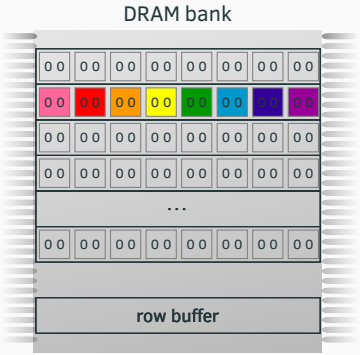


4 pages per row

Results

Row sharing

Sky Lake /w 2 DIMM



8 pages per row

Row sharing

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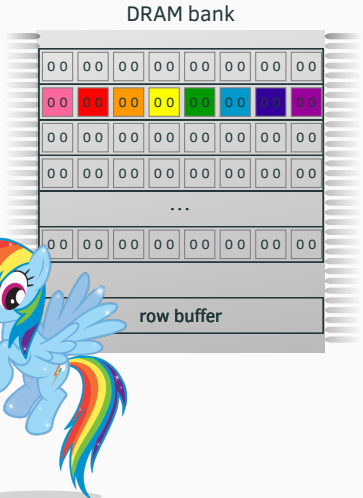

8 pages per row

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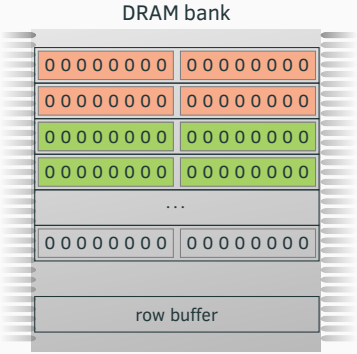
- For example, we can spy on keyboard inputs to Firefox

But Wait!!!---That's NOT All

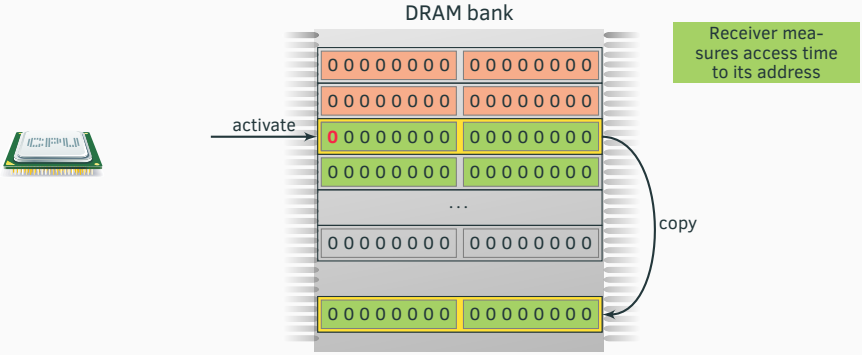
DRAM Covert Channel

Attack Primitive: Row miss



Sender and receiver decide on one bank

Attack Primitive: Row miss



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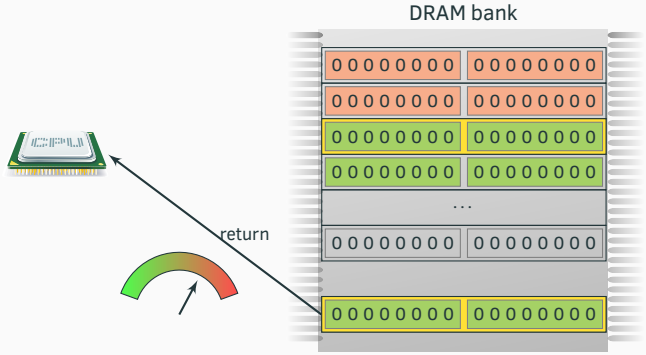

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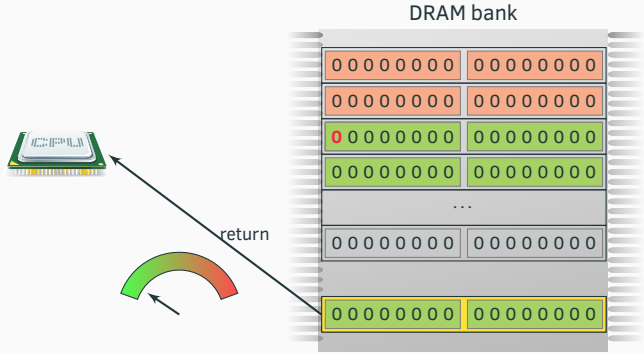
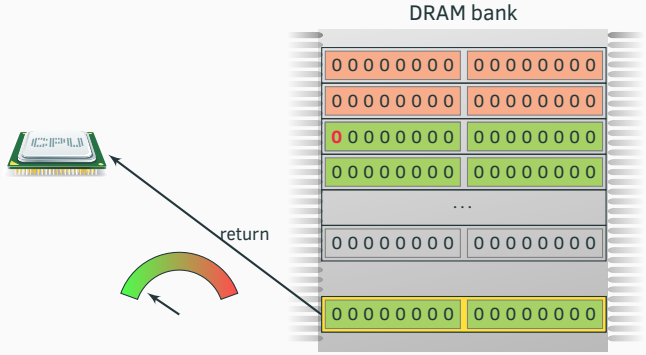


Repeated access always has low access times

Attack Primitive: Row miss



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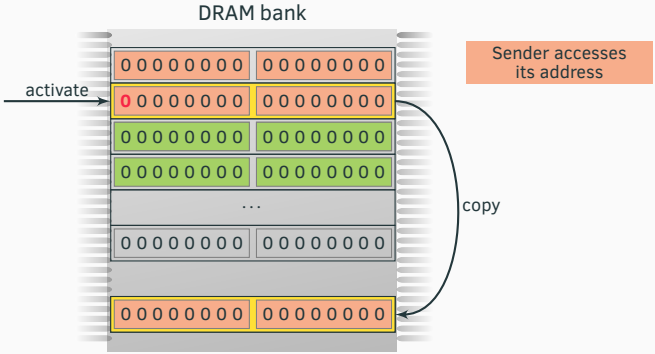

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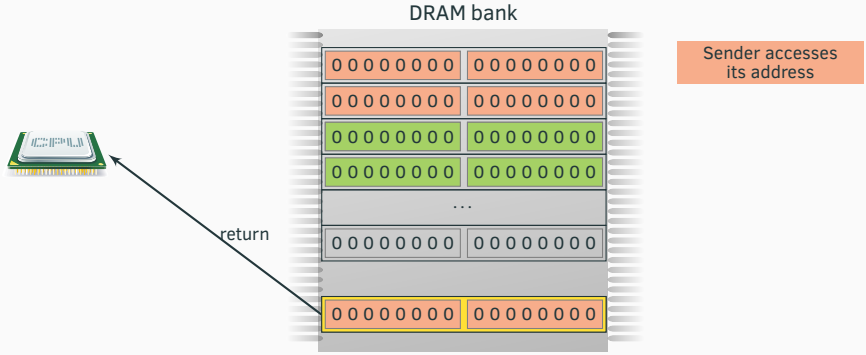

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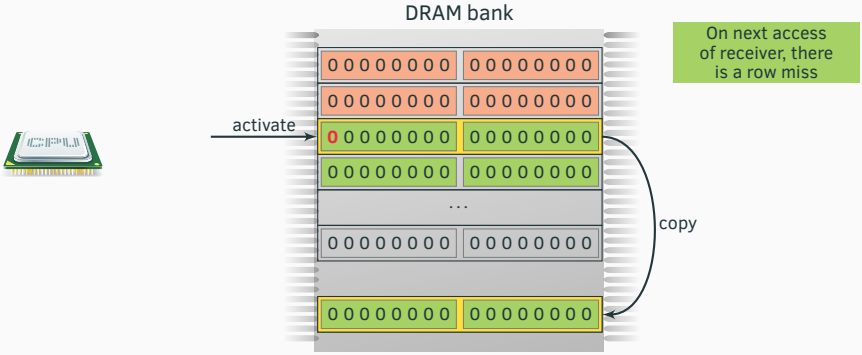

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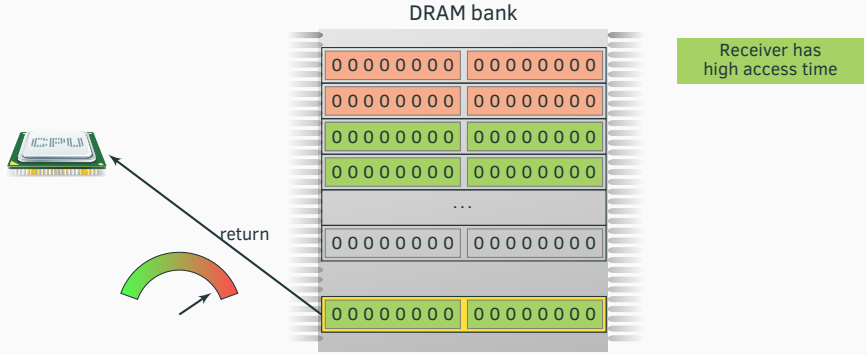

How our demo really works

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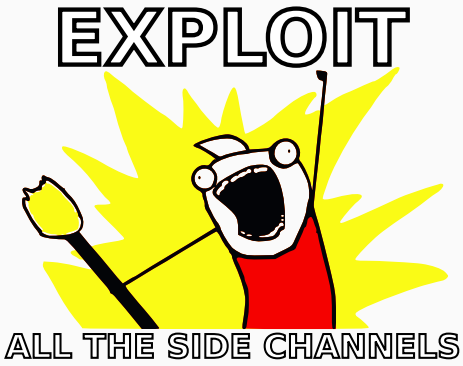

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We are “trapped” inside a VM without network hardware

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Scenario

We are “trapped” inside a VM without network hardware

- There is no communication between guest and host
- We want to get data out of the VM
- We cannot run binaries on the host system
- There are no known software bugs in either host, guest or virtualization software

The solution

The solution

A covert channel implemented in JavaScript

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- DRAM as side channel (main memory is “shared” between host and guest)

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A covert channel implemented in JavaScript

- DRAM as side channel (main memory is “shared” between host and guest)
- Sender inside the VM
- JavaScript running in the browser on the host
- We only have to trick the victim to visit our page

The gory details - bits

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The gory details - bits

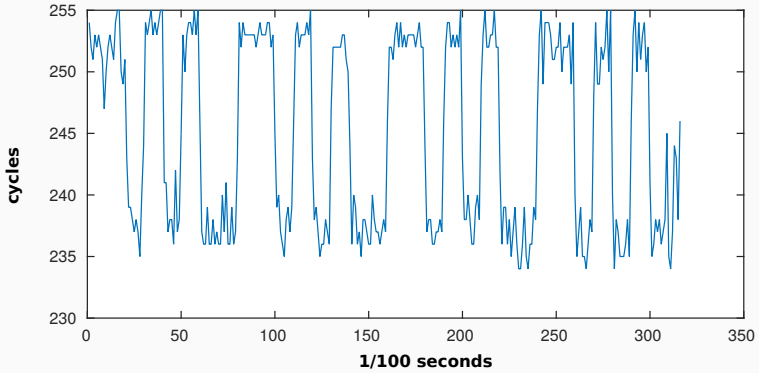

Figure 3: Multiple measurements per bit to have a reliable detection.

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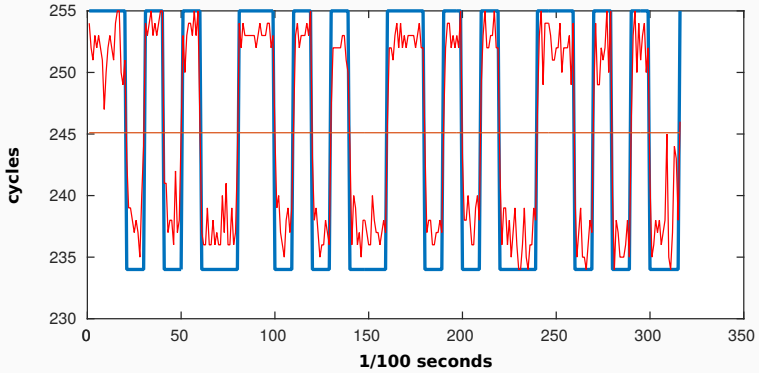

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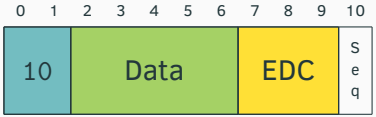

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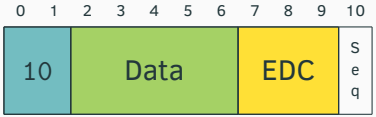
The gory details - Packets



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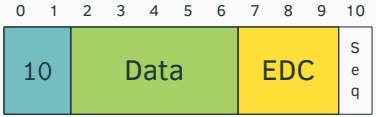

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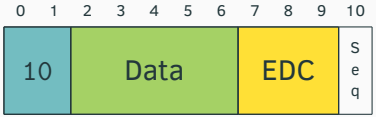

- Communication is based on packets
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- Data integrity is checked by an error-detection code (EDC)
- Sequence bit indicates whether it is a retransmission or a new packet

Results

- Transmission of approximately $11\ \text{bits/s}$

Results

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- Can be improved using

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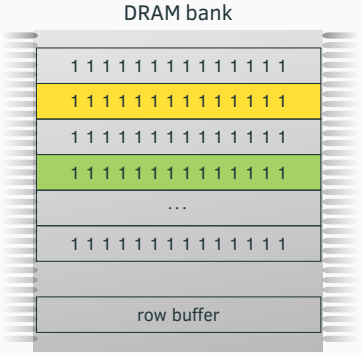
- Can be improved using
  - Fewer retransmits
  - Error correction
  - Multithreading $\rightarrow$ multiple banks in parallel
  - What is possible in native code? $596\,\mathrm{kbit/s}$ cross CPU and cross VM

Rowhammer

Rowhammer



- Capacitors leak $\rightarrow$ refresh necessary
- cells leak faster upon proximate accesses
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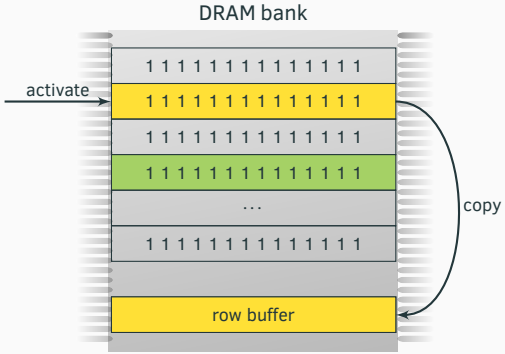

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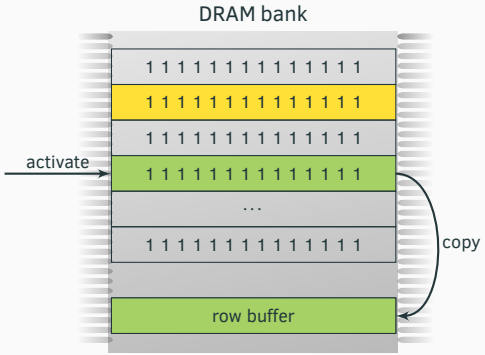

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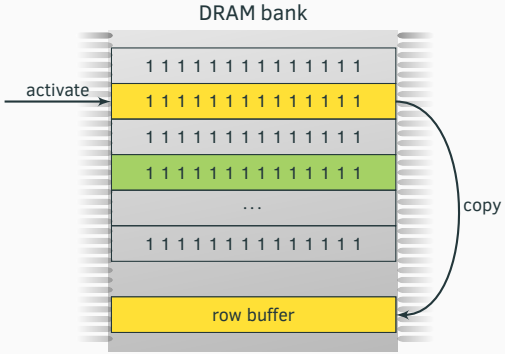

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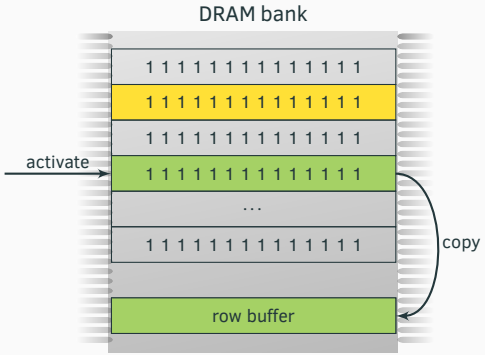

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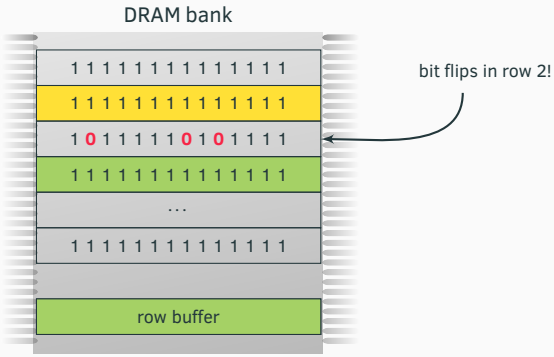

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Finding rows

The problem: Finding the victim row and the neighboring rows.

Finding rows

Solution 1: Spraying - We can fill memory with security relevant information and hammer randomly

- Seaborn 2015
- Spraying PTE and NaCl sanity checking code
- Problem: Not everything can be sprayed.

Finding rows

Solution 2: Deduplication

- Razavi et al. 2016
- We can have the operating system / hypervisor copy relevant information to a known location
- Problem: Deduplication is turned off in ”serious” cloud and default off in most operating systems.

Finding rows

Solution 3: Locate data - DRAMA: We know the mapping function

- Bhattacharya and Mukhopadhyay 2016
- Cool: We can now target row hammer
- Problem: Physical addresses.

Finding rows

Solution 3: Locate data - DRAMA: We know the mapping function

- Bhattacharya and Mukhopadhyay 2016
- Cool: We can now target row hammer
- Problem: Physical addresses.
- /proc/PID/pagemap
- cite prefetch
- Other leaks: ex. large pages and cache set congruency.

DDR4 Row hammer

Knowning the mapping funcion and physical address is what enabled bit flips in DDR4

Finding rows

Solution 4: Locate data - DRAMA: Row hits and misses

- If we can invoke victim:
- We can use row miss primitive to locate the bank
- We can use row hits primitive to locate rows

Finding rows

Solution 4: Locate data - DRAMA: Row hits and misses

- If we can invoke victim:
- We can use row miss primitive to locate the bank
- We can use row hits primitive to locate rows
- This is not perfect,
- but we can drastically improve accuracy

Conclusion

Black Hat Sound Bytes

Black Hat Sound Bytes.

- DRAM design is security relevant
- We can covertly exfiltrate information
- We can spy on other software
- We enable targeted row hammer attacks

References

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DRAMA: How your DRAM becomes a security problem

Michael Schwarz and Anders Fogh

November 4, 2016