X Factor:
Das Unfassbare

Die Geschichte von
Meltdown und Spectre

Michael Schwarz
(@misc0110)

Introduction

Is this all a conspiracy?

- Vulnerability existed for many years

Timeline of a Vulnerability

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- Vulnerability existed for many years
- No one discovered it before

Timeline of a Vulnerability

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Timeline of a Vulnerability

Is this all a conspiracy?

- Vulnerability existed for many years
- No one discovered it before
- Suddenly, 4 independent teams discover it within 6 months
- Let's create an evidence board


MANGARD
LIPP
GRUSS
SCHWARZ
TU
Graz


FOGH


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LIPP
GRUSS
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TU
Graz


FOGH
Academic?
Hacker?


MANGARD
LIPP
GRUSS
ICHWARZ
TU
Graz

Academic?
Hacker?

black hat

Academic?
Hacker?

black hat

ACM CCS 2016

Academic?
Hacker?

ACM
CCS
2016

Academic?
Hacker?

Meltdown

Academic?
Hacker?

black hat

ACM CCS 2016

Meltdown

Academic?
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black hat

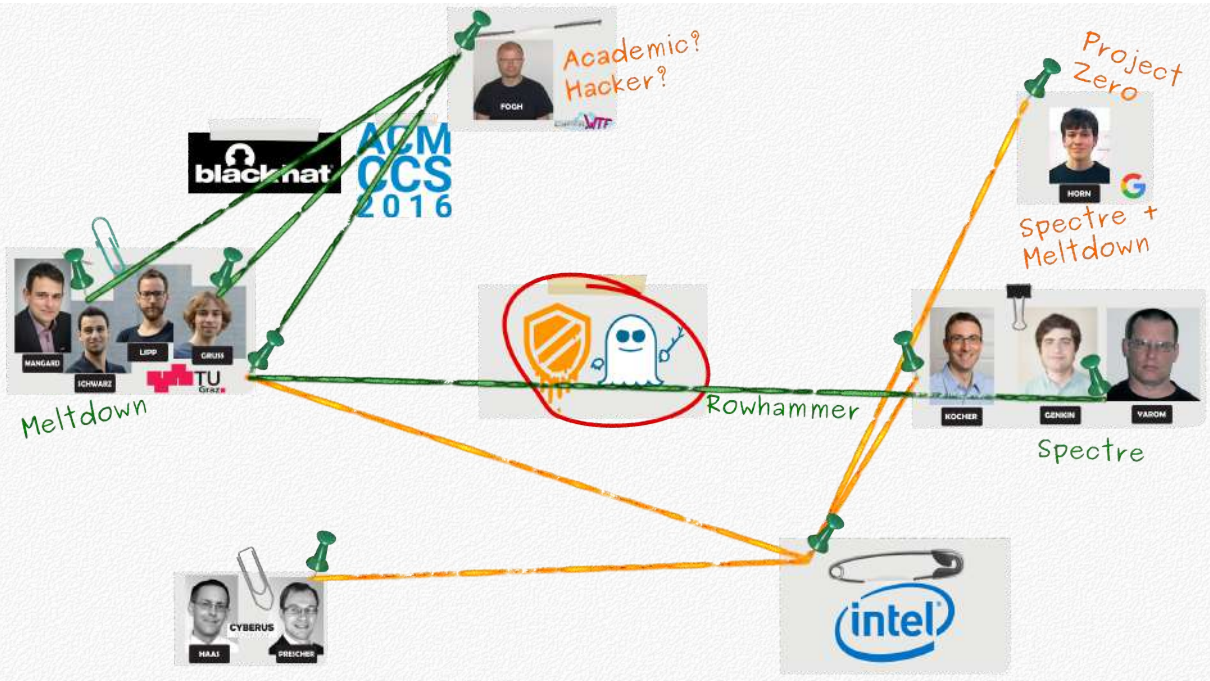
ACM CCS 2016

Meltdown

Project Zero

Spectre + Meltdown

Spectre


Academic?
Hacker?
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Zero
HORN
Spectre +
Meltdown
black hat
ACM
CCS
2016
MANGARD
LIPP
GRUSS
SCHWARZ
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Meltdown
Rowhammer
KOCHER
GENKIN
YAROM
Spectre
CYBERUS
HAAS
FREICHER
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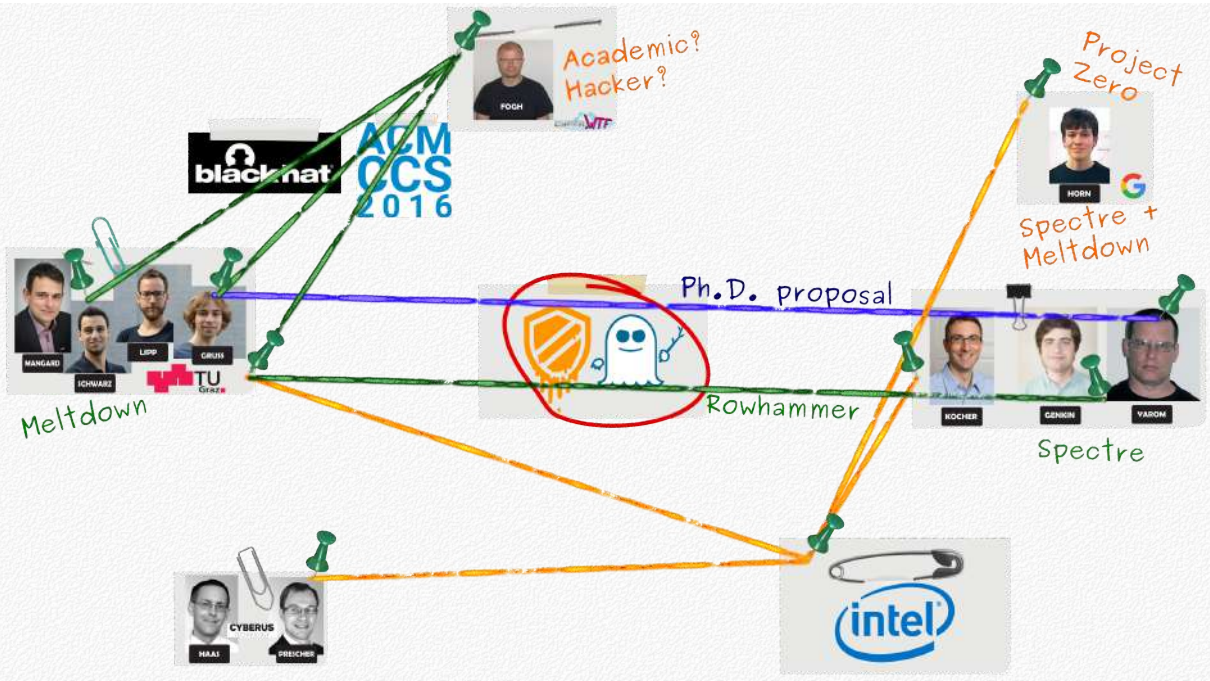
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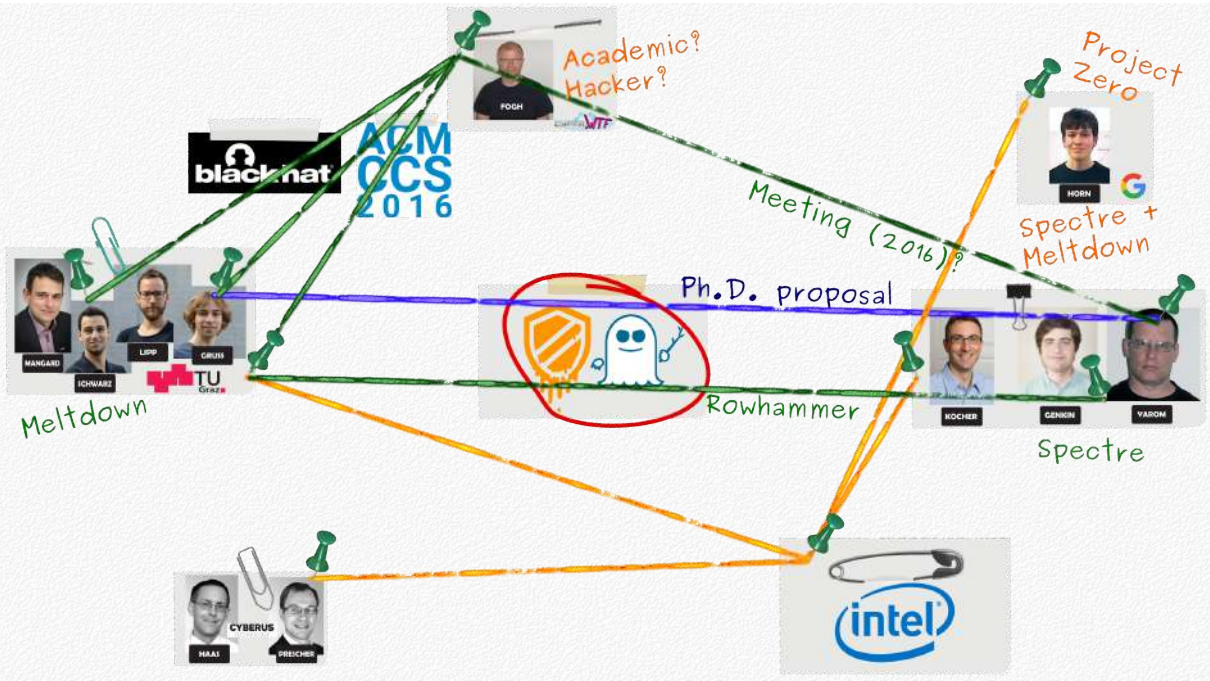
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Meeting (2016)?
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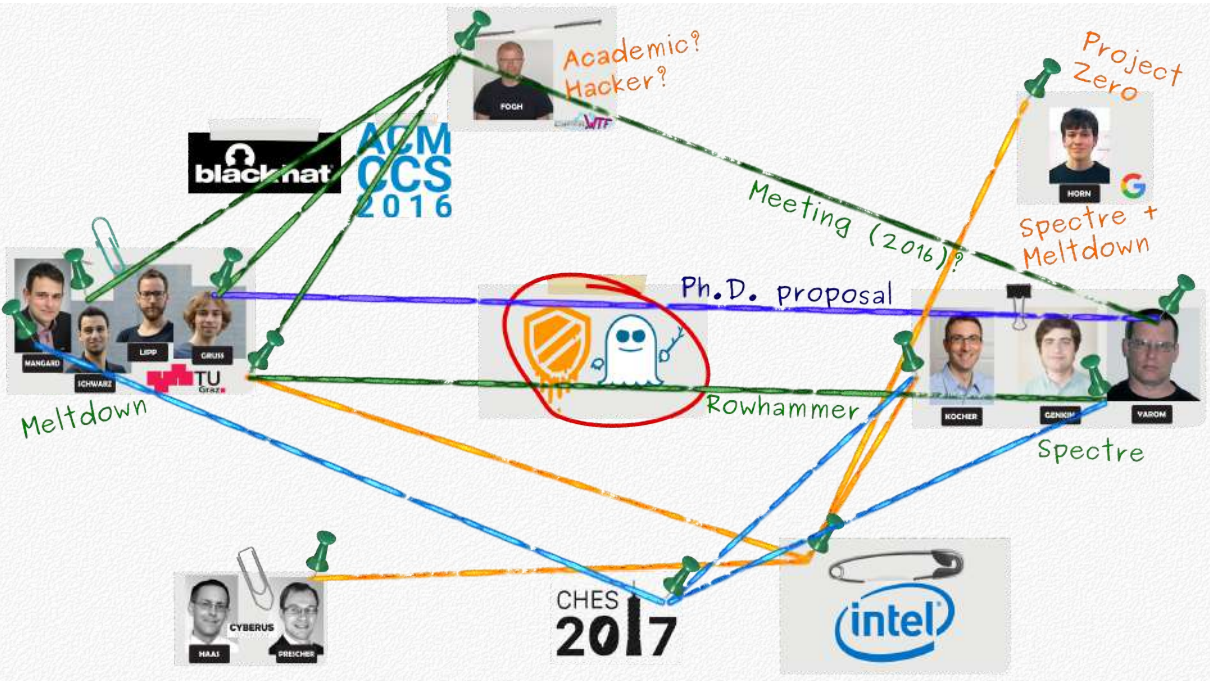
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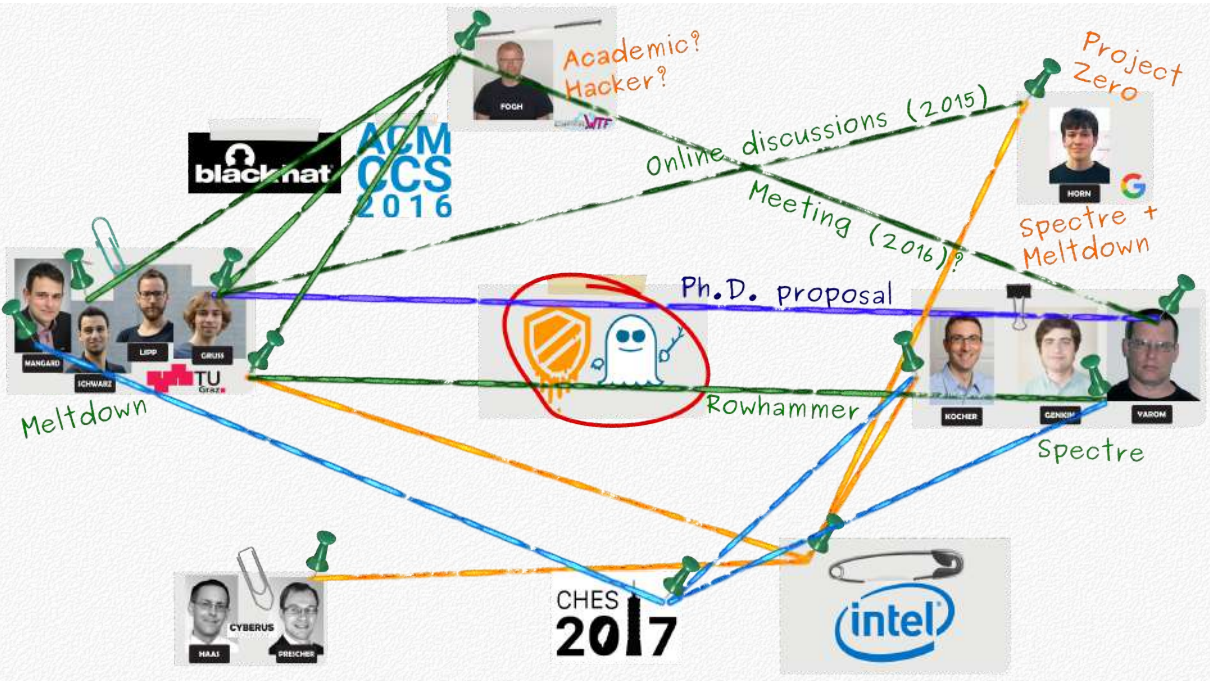
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Online discussions (2015)
Meeting (2016)?
HORN
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GENKIN
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CHES
2017
intel

Not a conspiracy

- Tools to detect the bug only invented in 2014

Timeline of a Vulnerability

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- No broad interest in microarchitectural attacks before

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- The bug was “ripe” $\Rightarrow$ a consequence of research in this area

Timeline of a Vulnerability

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- Discovering teams quite knowledgeable in this area
- The bug was “ripe” $\Rightarrow$ a consequence of research in this area

$\rightarrow$ bug collision nearly inevitable

The Fallout

You realize it is something big when...

The Fallout

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- it is in the news, all over the world


WASHINGTON, D.C.
FOX
BUSINESS
WASHINGTON, D.C.
WINTER STORM
NEWS
› ALERT
INTEL REVEALS DESIGN FLAW THAT
COULD ALLOW HACKERS TO ACCESS DATA
FOX
BUSINESS
NETWORK
@FOXBUSINESS


FIREEYE CYBER
THREAT MAP
DEVELOPING STORY
COMPUTER CHIP FLAWS IMPACT BILLIONS OF DEVICES
LIVE
CNN
DAX ▲164.69
NEWS STREAM


GLOBAL
COMPUTER CHIP SCARE
The bugs are known as 'Spectre' and 'Meltdown'
BBC WORLD NEWS
£:HK$ 10.58
EURO:£ 0.891


SECURITY FLAW REVEALED
Intel (Prev)
45.26
-1.59
[-3.39%]
Intel (After Hours)
44.85
-0.41
[-0.91%]
CAPITAL CONNECTION
SHROUT: ISSUE NOT UNIQUE TO INTEL, BUT IT'S AFFECTED THE MOST
CNBC

The Fallout

You realize it is something big when...

- it is in the news, all over the world
- you get a Wikipedia article in multiple languages

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Meltdown (security vulnerability)

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Meltdown is a hardware vulnerability affecting Intel x86 microprocessors and some ARM-based microprocessors.[1][2][3] It allows a rogue process to read all memory, even when it is not authorized to do so.

Meltdown affects a wide range of systems. At the time of disclosure, this included all devices running any but the most recent and patched versions of iOS,[4] Linux[5][6], macOS,[4] or Windows. Accordingly, many servers and cloud services were impacted,[7] as well as a potential majority of smart devices and embedded devices using ARM based processors (mobile devices, smart TVs and others), including a wide range of networking equipment. A purely software workaround to Meltdown has been assessed as slowing computers between 5 and 30 percent in certain specialized workloads,[8] although companies responsible for software correction of the exploit are reporting minimal impact from general benchmark testing.[9]

Meltdown was issued a Common Vulnerabilities and Exposures ID of CVE-2017-5754, also known as *Rogue Data Cache Load*,[2] in January 2018. It was disclosed in conjunction with another exploit, Spectre, with which it shares some, but not all characteristics. The Meltdown and Spectre vulnerabilities are considered "catastrophic"

The logo used by the team that discovered the vulnerability

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Spectre (security vulnerability)

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Spectre is a vulnerability that affects modern microprocessors that perform branch prediction.[1][2][3] On most processors, the speculative execution resulting from a branch misprediction may leave observable side effects that may reveal private data to attackers. For example, if the pattern of memory accesses performed by such speculative execution depends on private data, the resulting state of the data cache constitutes a side channel through which an attacker may be able to extract information about the private data using a timing attack.[4][5][6]

A logo created for the vulnerability, featuring a ghost with a branch

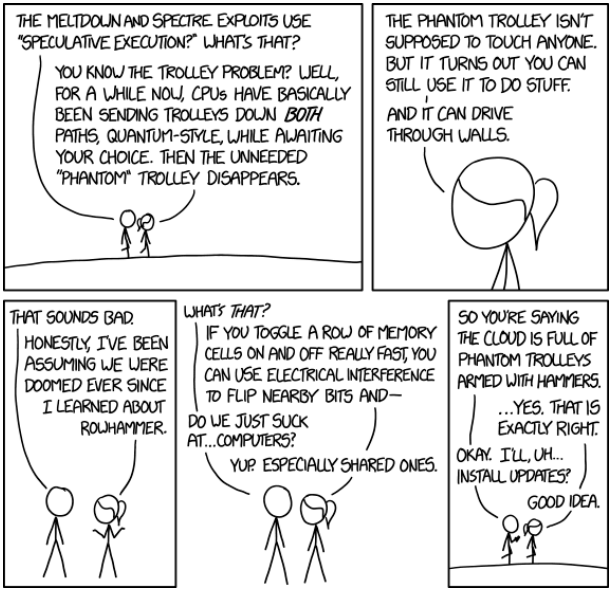
Two Common Vulnerabilities and Exposures IDs related to Spectre, CVE-2017-5753 (bounds check bypass) and CVE-2017-5715 (branch target injection), have been issued.[7] JIT engines used for JavaScript were found vulnerable. A website can read data stored in the browser for another website, or the browser's memory itself.[8]

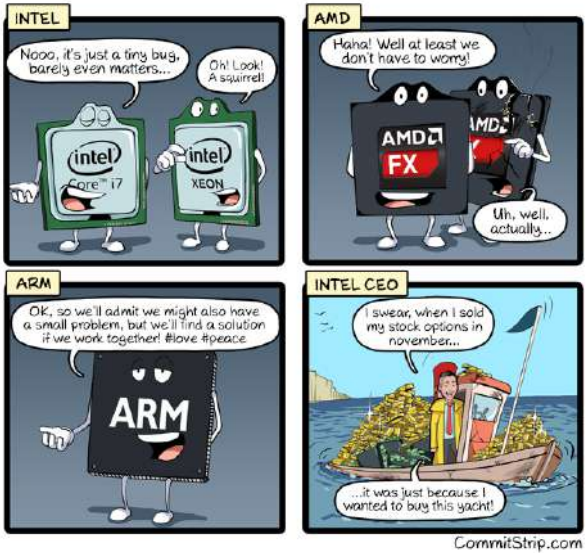
Several procedures to help protect home computers and related devices from the Spectre (and Meltdown) security vulnerabilities have been published.[9][10][11][12] Spectre patches have been reported to significantly slow down performance, especially on older computers; on the newer 8th generation Core platforms, benchmark performance drops of 2–14 percent have been measured.[13] Meltdown patches may also produce performance loss.[5][14][15] On January 18, 2018, unwanted reboots, even for newer Intel chips, due to

The Fallout

You realize it is something big when...

- it is in the news, all over the world
- you get a Wikipedia article in multiple languages
- there are comics, including xkcd

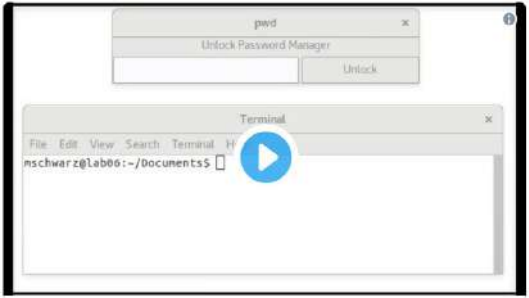

THE MELTDOWN AND SPECTRE EXPLOITS USE "SPECULATIVE EXECUTION?" WHAT'S THAT?
YOU KNOW THE TROLLEY PROBLEM? WELL, FOR A WHILE NOW, CPUs HAVE BASICALLY BEEN SENDING TROLLEYS DOWN BOTH PATHS, QUANTUM-STYLE, WHILE AWAITING YOUR CHOICE. THEN THE UNNEEDED "PHANTOM" TROLLEY DISAPPEARS.
THE PHANTOM TROLLEY ISN'T SUPPOSED TO TOUCH ANYONE. BUT IT TURNS OUT YOU CAN STILL USE IT TO DO STUFF.
AND IT CAN DRIVE THROUGH WALLS.
THAT SOUNDS BAD.
HONESTLY, I'VE BEEN ASSUMING WE WERE DOOMED EVER SINCE I LEARNED ABOUT ROWHAMMER.
WHAT'S THAT?
IF YOU TOGGLE A ROW OF MEMORY CELLS ON AND OFF REALLY FAST, YOU CAN USE ELECTRICAL INTERFERENCE TO FLIP NEARBY BITS AND—
DO WE JUST SUCK AT...COMPUTERS?
YUP. ESPECIALLY SHARED ONES.
SO YOU'RE SAYING THE CLOUD IS FULL OF PHANTOM TROLLEYS ARMED WITH HAMMERS.
...YES. THAT IS EXACTLY RIGHT.
OKAY. I'LL, UH... INSTALL UPDATES?
GOOD IDEA.


INTEL
Nooo, it's just a tiny bug, barely even matters...
Oh! Look! A squirrel!
intel
Core™ i7
intel
XEON
AMD
Haha! Well at least we don't have to worry!
AMD
FX
Uh, well, actually...
ARM
Ok, so we'll admit we might also have a small problem, but we'll find a solution if we work together! #love #peace
ARM
INTEL CEO
I swear, when I sold my stock options in november...
...it was just because I wanted to buy this yacht!
CommitStrip.com

The Fallout

You realize it is something big when...

- it is in the news, all over the world
- you get a Wikipedia article in multiple languages
- there are comics, including xkcd
- you get a lot of Twitter follower after Snowden mentioned you



Edward Snowden
@Snowden

You may have heard about @Intel's horrific #Meltdown bug. But have you watched it in action? When your computer asks you to apply updates this month, don't click "not now." (via spectreattack.com & @misc0110)

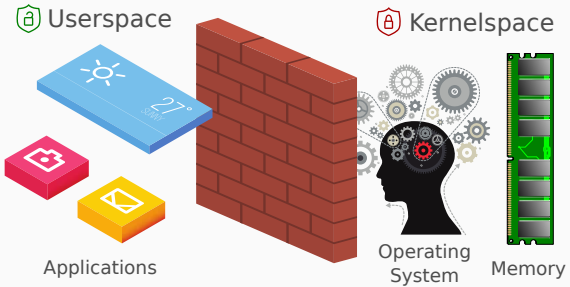
23:37 - 4. Jan. 2018

152 6.547 6.512

MELTDOWN

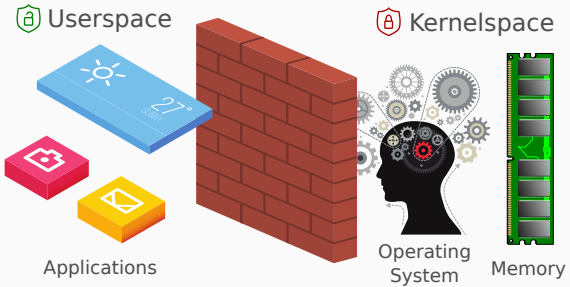
The Core of Meltdown

- Kernel is isolated from user space



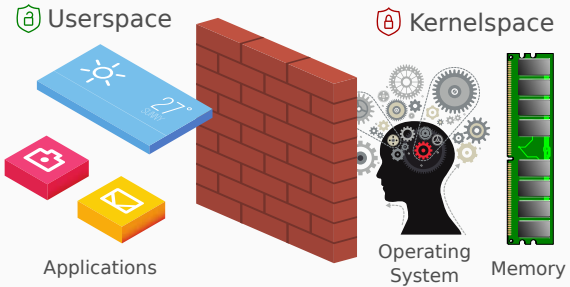
The Core of Meltdown

- Kernel is isolated from user space
- This isolation is a combination of hardware and software



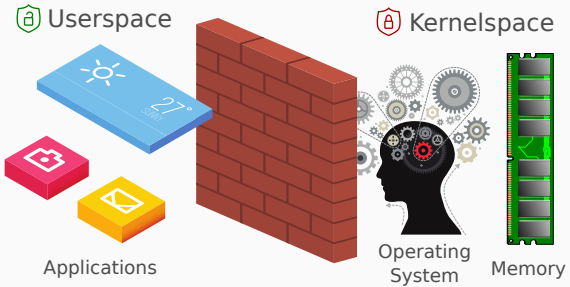
The Core of Meltdown

- Kernel is isolated from user space
- This isolation is a combination of hardware and software
- User applications cannot access anything from the kernel

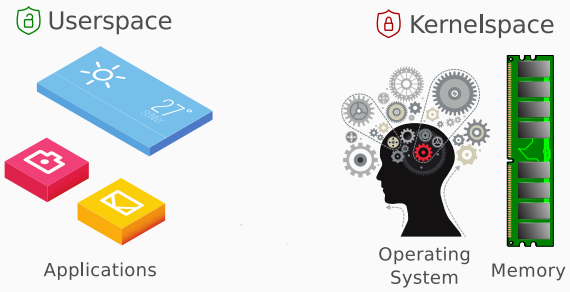


The Core of Meltdown

- Kernel is isolated from user space
- This isolation is a combination of hardware and software
- User applications cannot access anything from the kernel
- There is only a well-defined interface → syscalls

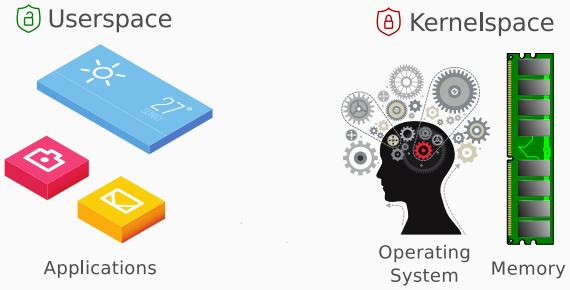


- Breaks isolation between applications and kernel



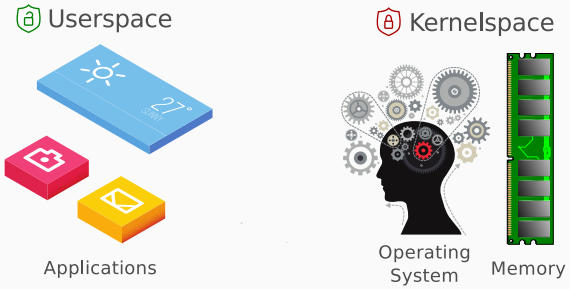
Meltdown Briefing

- Breaks isolation between applications and kernel
- User applications can access kernel addresses



Meltdown Briefing

- Breaks isolation between applications and kernel
- User applications can access kernel addresses
- Entire physical memory is mapped in the kernel



Meltdown Briefing

- Breaks isolation between applications and kernel
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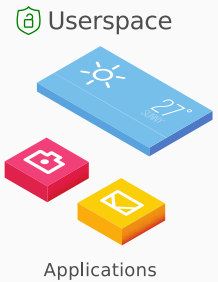
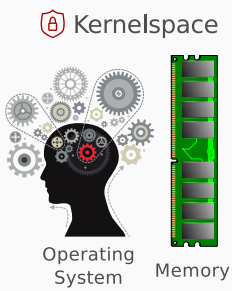
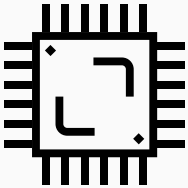
- Entire physical memory is mapped in the kernel

→ Meltdown can read whole DRAM



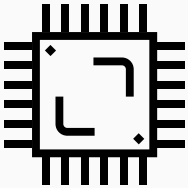


Meltdown Requirements



- Only on Intel CPUs and some ARMs (Cortex A75)

Meltdown Requirements



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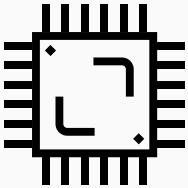

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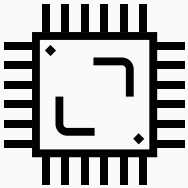

- Only on Intel CPUs and some ARMs (Cortex A75)
- AMD and other ARMs seem to be unaffected
- Common cause: permission check done in parallel to load instruction
- Race condition between permission check and dependent operation(s)

1337 4242

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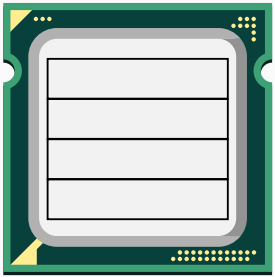
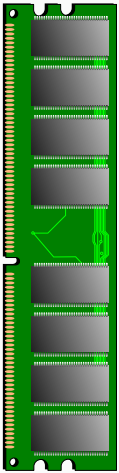
CPU Cache

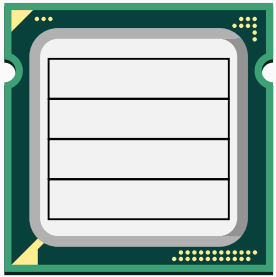
```
printf("%d", i);
printf("%d", i);
```

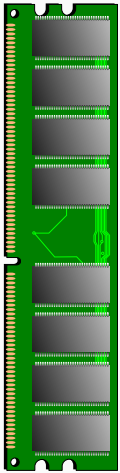




```
printf("%d", i);
printf("%d", i);
```

Cache miss





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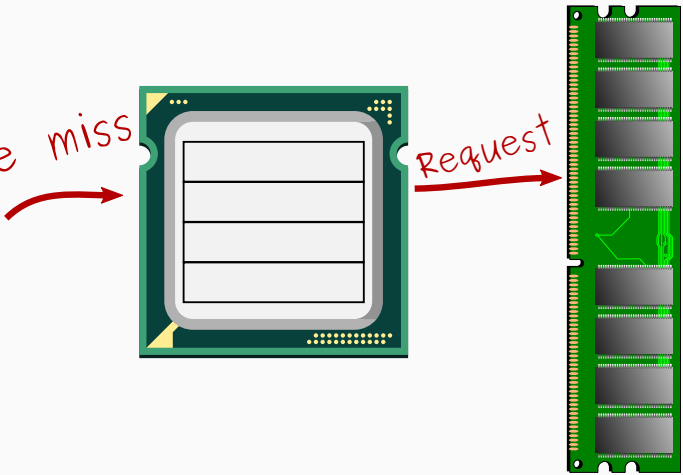

```
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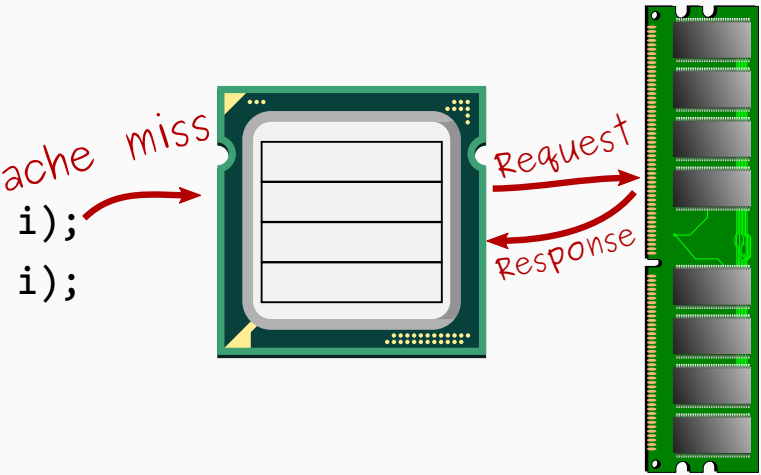

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```
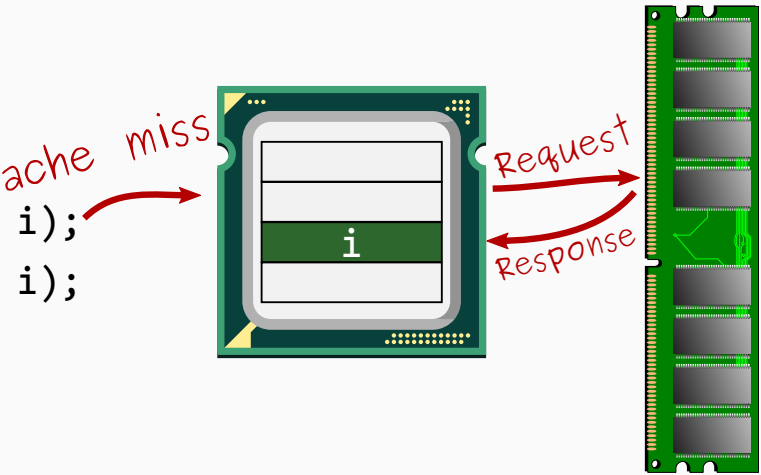
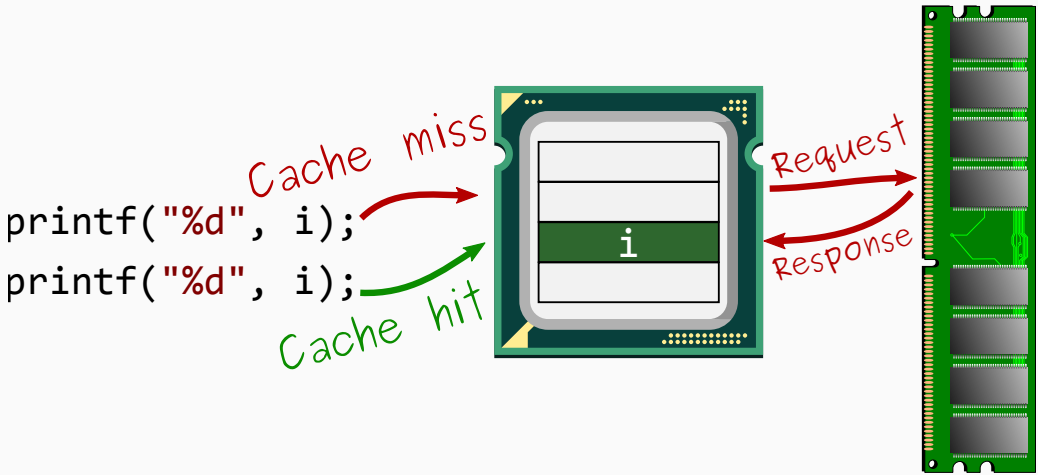
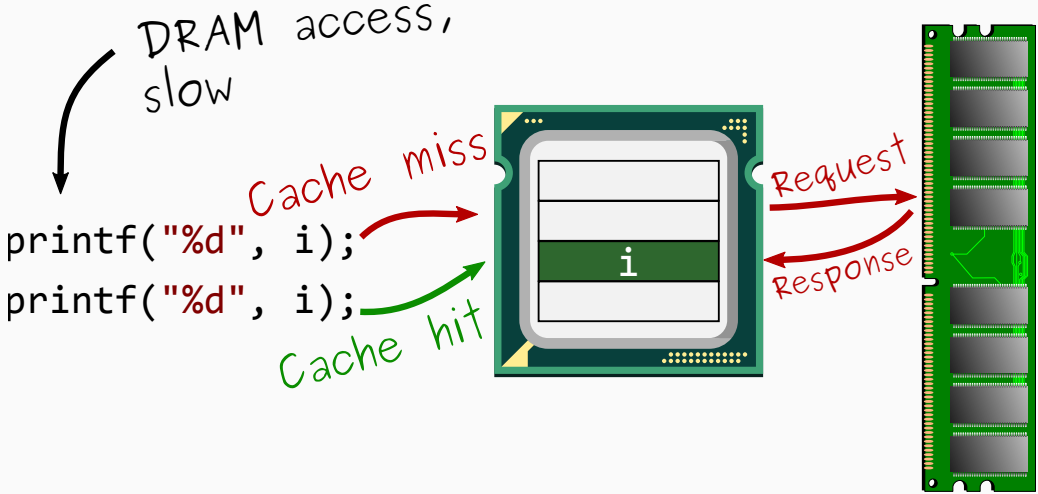
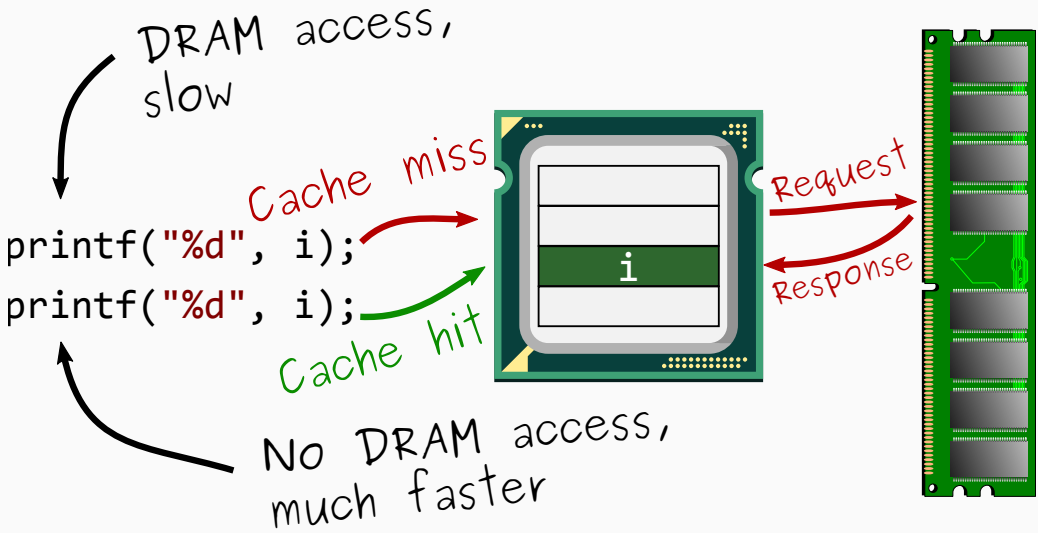




printf("%d", i);
printf("%d", i);
Cache miss
Cache hit
i
Request
Response


DRAM access, slow
printf("%d", i);
printf("%d", i);
Cache miss
Cache hit
i
Request
Response

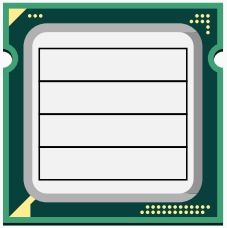

DRAM access, slow
printf("%d", i);
printf("%d", i);
Cache miss
Cache hit
i
Request
Response
No DRAM access, much faster

Shared Memory

ATTACKER

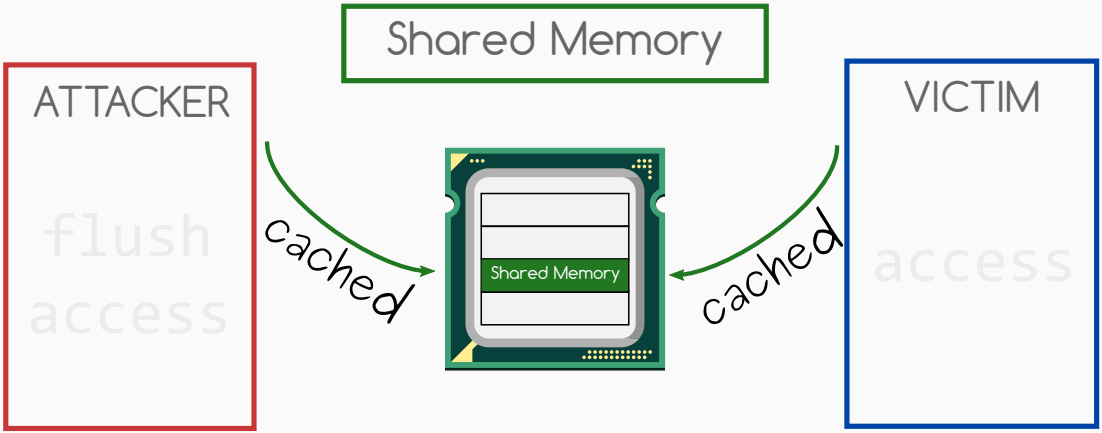
flush

access



VICTIM

access

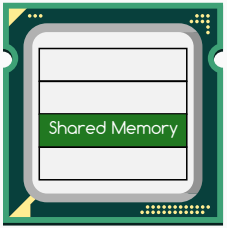

Shared Memory
ATTACKER
flush
access
cached
Shared Memory
cached
VICTIM
access

Shared Memory

ATTACKER

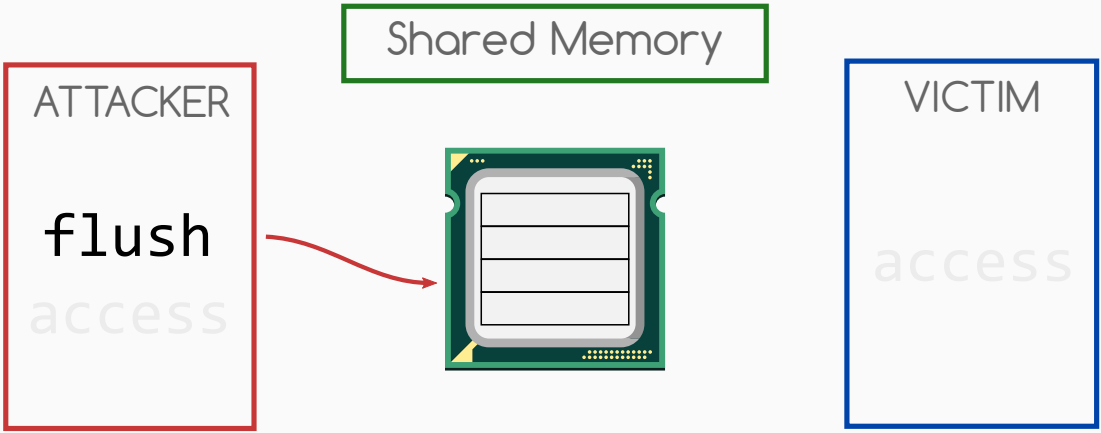
flush

access



VICTIM

access

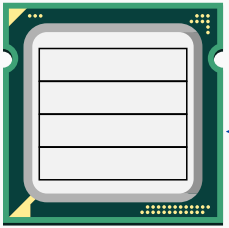

Shared Memory
ATTACKER
flush
access
VICTIM
access

Shared Memory

ATTACKER

flush

access



VICTIM

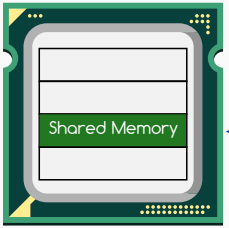
access

Shared Memory

ATTACKER

flush

access



VICTIM

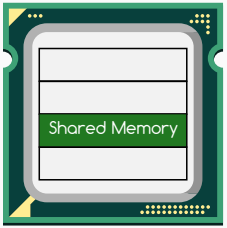
access

Shared Memory

ATTACKER

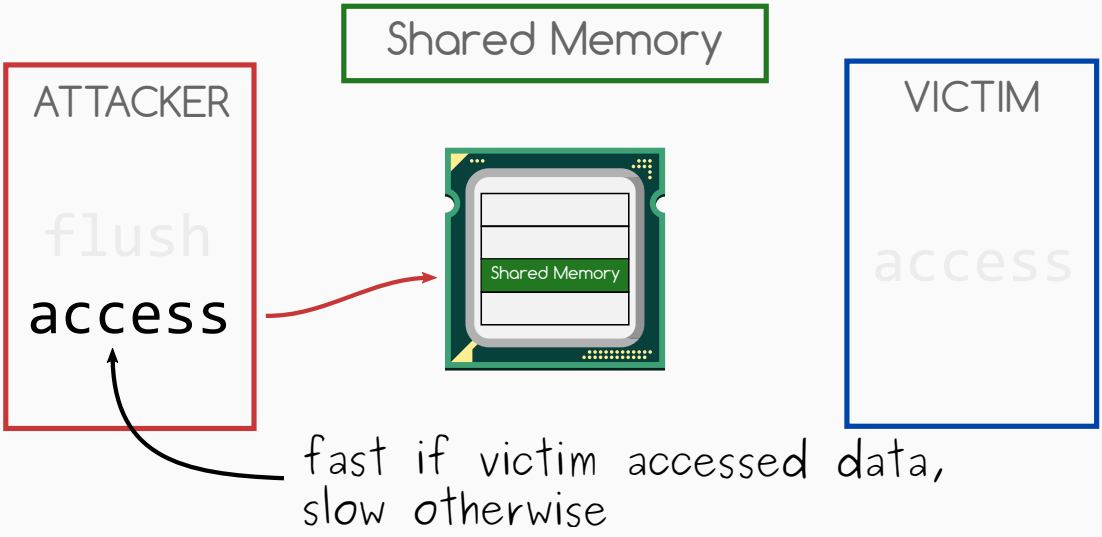
flush

access



VICTIM

access


Shared Memory
ATTACKER
flush
access
Shared Memory
VICTIM
access
fast if victim accessed data,
slow otherwise

Back to Work

7. Serve with cooked and peeled potatoes

Wait for an hour

Wait for an hour

LATENCY

1. Wash and cut vegetables

2. Pick the basil leaves and set aside

3. Heat 2 tablespoons of oil in a pan

4. Fry vegetables until golden and softened

Dependency

1. Wash and cut vegetables

2. Pick the basil leaves and set aside

3. Heat 2 tablespoons of oil in a pan

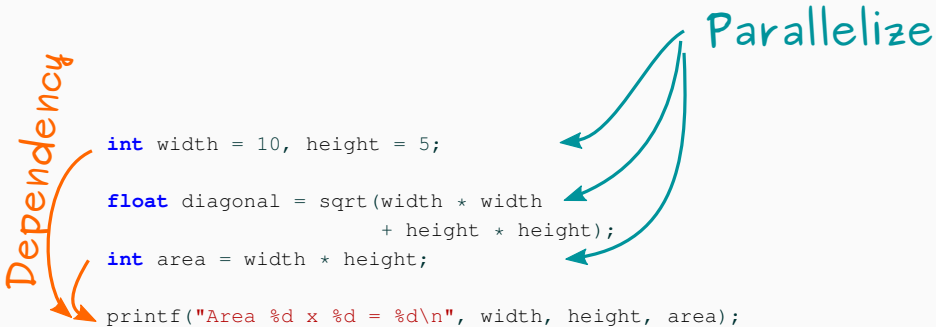
4. Fry vegetables until golden and softened

Parallelize

Out-of-order Execution

```
int width = 10, height = 5;

float diagonal = sqrt(width * width
                      + height * height);
int area = width * height;

printf("Area %d x %d = %d\n", width, height, area);
```

Out-of-order Execution



Building the Code

- Find something human readable, e.g., the Linux version

```
# sudo grep linux_banner /proc/kallsyms
ffffffff81a000e0 R linux_banner
```

```
char data = *(char*)0xffffffff81a000e0;
printf("%c\n", data);
```

- Compile and run

```
segfault at ffffffff81a000e0 ip 0000000000400535
            sp 00007ffce4a80610 error 5 in reader
```

Building the Code

- Compile and run

```
segfault at ffffffff81a000e0 ip 0000000000400535
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- Kernel addresses are of course not accessible

- Compile and run

```
segfault at ffffffff81a000e0 ip 0000000000400535
            sp 00007ffce4a80610 error 5 in reader
```

- Kernel addresses are of course not accessible
- Any invalid access throws an exception → segmentation fault

Building the Code

- Just catch the segmentation fault!

- Just catch the segmentation fault!
- We can simply install a signal handler

Building the Code

- Just catch the segmentation fault!
- We can simply install a signal handler
- And if an exception occurs, just jump back and continue

Building the Code

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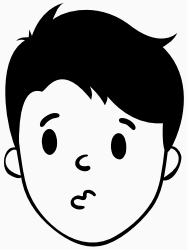
- And if an exception occurs, just jump back and continue
- Then we can read the value

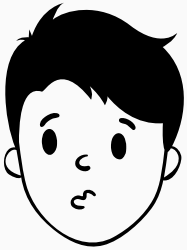
- Just catch the segmentation fault!
- We can simply install a signal handler
- And if an exception occurs, just jump back and continue
- Then we can read the value
- Sounds like a good idea

Building the Code



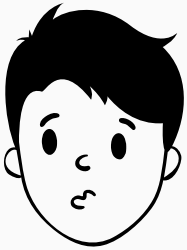
- Still no kernel memory

Building the Code



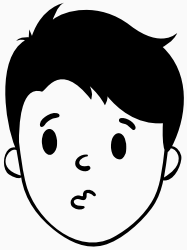
- Still no kernel memory
- Maybe it is not that straight forward

Building the Code



- Still no kernel memory
- Maybe it is not that straight forward
- Privilege checks seem to work

Building the Code



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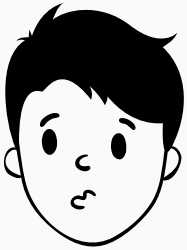
- Privilege checks seem to work
- Are privilege checks also done when executing instructions out of order?

Building the Code



- Still no kernel memory
- Maybe it is not that straight forward
- Privilege checks seem to work
- Are privilege checks also done when executing instructions out of order?
- Problem: out-of-order instructions are not visible

- Adapted code

```
*(volatile char*)0;
array[84 * 4096] = 0;
```

Building the Code

- Adapted code

```
*(volatile char*)0;
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```

- `volatile` because compiler was not happy

```
warning: statement with no effect [-Wunused-value]
         *(char*)0;
```

- Adapted code

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*(volatile char*)0;
array[84 * 4096] = 0;
```

- `volatile` because compiler was not happy

```
warning: statement with no effect [-Wunused-value]
         *(char*)0;
```

- Static code analyzer is still not happy

```
warning: Dereference of null pointer
         *(volatile char*)0;
```

- Flush+Reload over all pages of the array

- "Unreachable" code line was actually executed

- Flush+Reload over all pages of the array

- "Unreachable" code line was actually executed
- Exception was only thrown afterwards

Building the Code

- Out-of-order instructions leave microarchitectural traces

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- We can see them for example in the cache

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- Give such instructions a name: transient instructions

Building the Code

- Out-of-order instructions leave microarchitectural traces
- We can see them for example in the cache
- Give such instructions a name: transient instructions
- We can indirectly observe the execution of transient instructions

- Maybe there is no permission check in transient instructions...

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- ...or it is only done when commiting them

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- Add another layer of indirection to test

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```

- Maybe there is no permission check in transient instructions...
- ...or it is only done when commiting them
- Add another layer of indirection to test

```
char data = *(char*)0xffffffff81a000e0;
array[data * 4096] = 0;
```

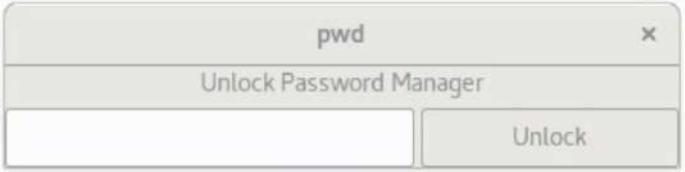
- Then check whether any part of `array` is cached

- Flush+Reload over all pages of the array

- Index of cache hit reveals data

- Flush+Reload over all pages of the array

- Index of cache hit reveals data
- Permission check is in some cases not fast enough



Terminal

File Edit View Search Terminal Help

```
mschwarz@lab06:~/Documents$
```

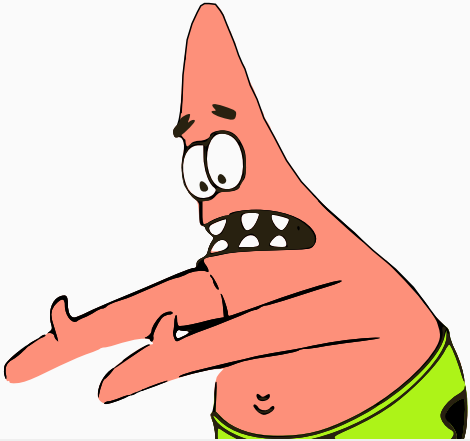
And now?...

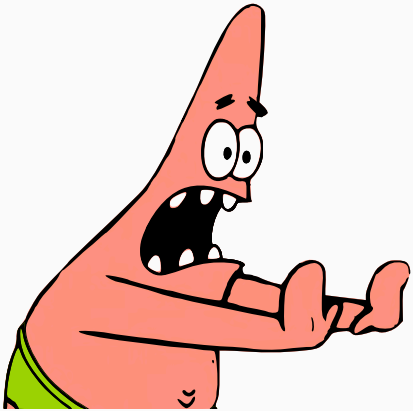
Take the kernel addresses...

- Kernel addresses in user space are a problem

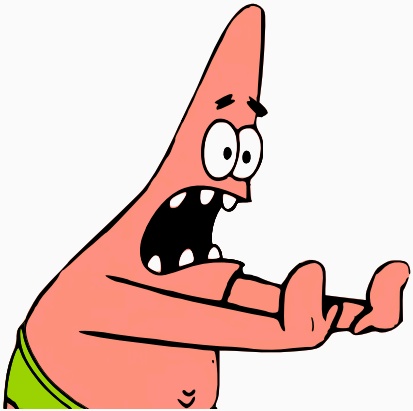
Take the kernel addresses...

- Kernel addresses in user space are a problem
- Why don't we take the kernel addresses...





- ...and remove them if not needed?



- ...and remove them if not needed?
- User accessible check in hardware is not reliable

Idea

- Let's just unmap the kernel in user space

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- Kernel addresses are then no longer present

Idea

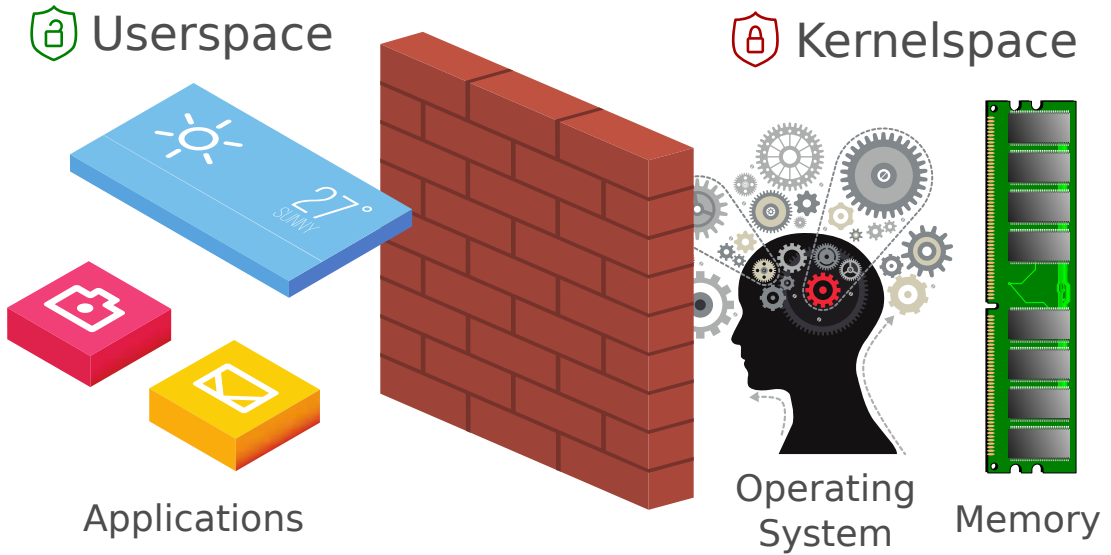
- Let's just unmap the kernel in user space
- Kernel addresses are then no longer present
- Memory which is not mapped cannot be accessed at all


Kernel Address Isolation to have Side channels Efficiently Removed

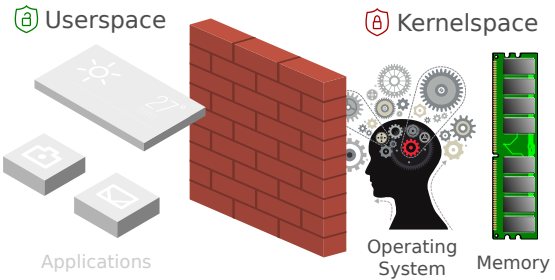
KAISER /ˈkʌɪzə/

1. [german] Emperor, ruler of an empire
2. largest penguin, emperor penguin

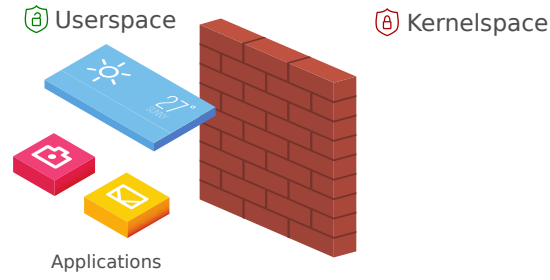
Kernel **A**ddress **I**solation to have **S**ide channels **E**fficiently **R**emoved

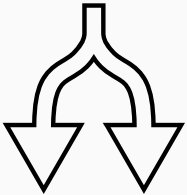

Userspace
Kernelspace
27°
Applications
Operating System
Memory

Kernel View



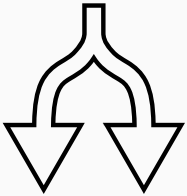
User View





- We published KAISER in July 2017

Kernel Address Space Isolation



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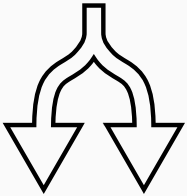
Kernel Address Space Isolation



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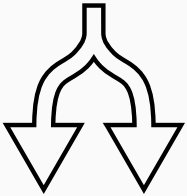

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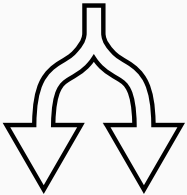
Kernel Address Space Isolation



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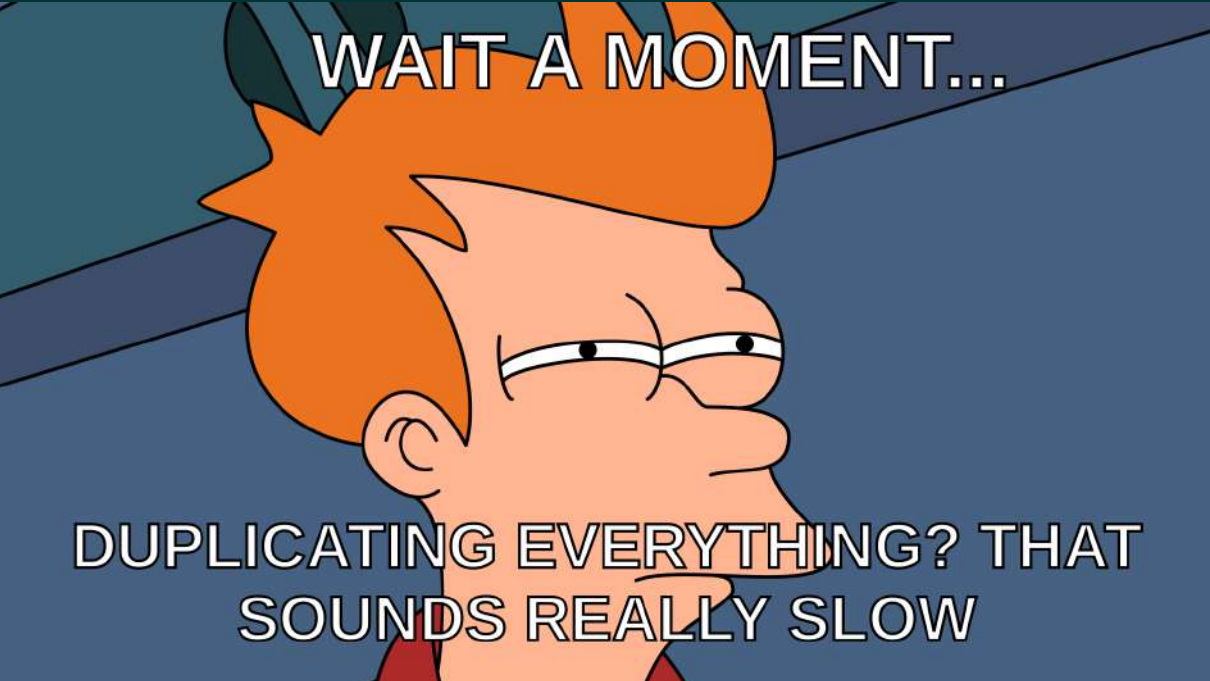
- Intel and others improved and merged it into Linux as KPTI (Kernel Page Table Isolation)
- Microsoft implemented similar concept in Windows 10
- Apple implemented it in macOS 10.13.2 and called it "Double Map"
- All share the same idea: switching address spaces on context switch


WAIT A MOMENT...
DUPLICATING EVERYTHING? THAT SOUNDS REALLY SLOW

Performance

- Depends on how often you need to switch between kernel and user space

Performance

- Depends on how often you need to switch between kernel and user space
- Can be slow, 40% or more on old hardware

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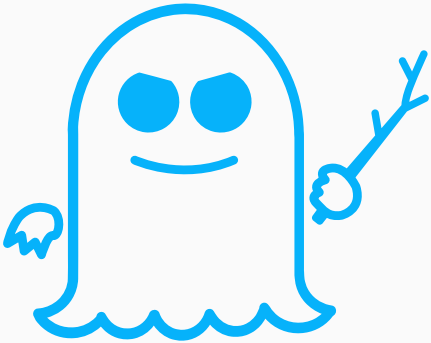
Performance

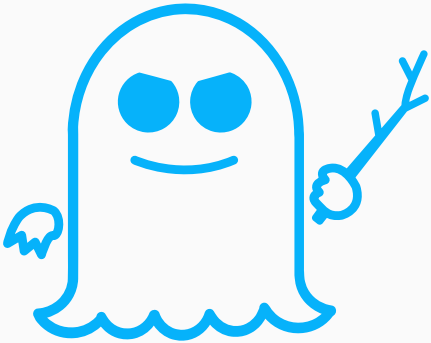
- Depends on how often you need to switch between kernel and user space
- Can be slow, 40% or more on old hardware
- But modern CPUs have additional features
- $\Rightarrow$ Performance overhead on average below 2%

MELTDOWN

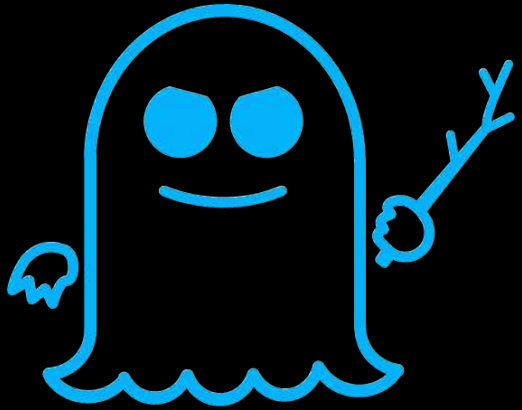


SPECTRE

MELTDOWN



SPECTRE



SPECTRE

- Mistrains branch prediction

Spectre Briefing

- Mistrains branch prediction
- CPU speculatively executes code which should not be executed

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- CPU speculatively executes code which should not be executed
- Can also mistrain indirect calls

Spectre Briefing

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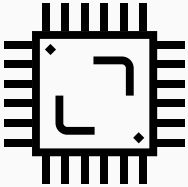
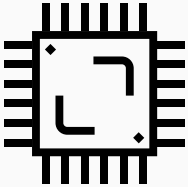
→ Spectre “convinces” program to execute code

Spectre Requirements



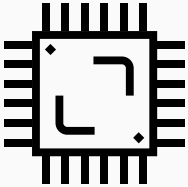
- On Intel and AMD CPUs

Spectre Requirements



- On Intel and AMD CPUs
- Some ARMs (Cortex R and Cortex A) are also affected

Spectre Requirements



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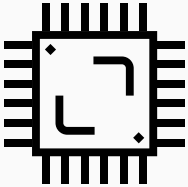
Spectre Requirements



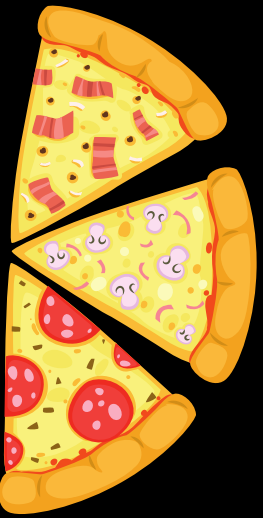
- On Intel and AMD CPUs
- Some ARMs (Cortex R and Cortex A) are also affected
- Common cause: speculative execution of branches
- Speculative execution leaves microarchitectural traces which leak secret

PIZZA

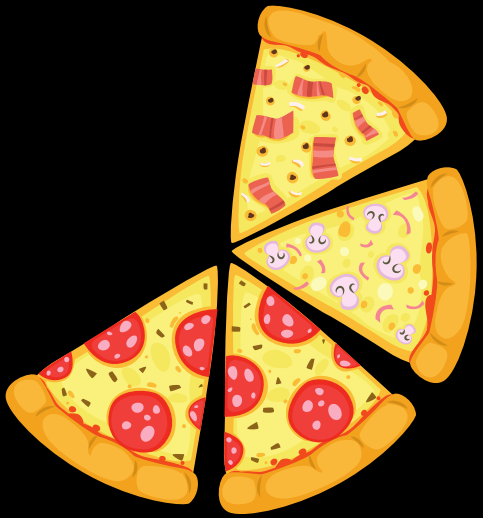
SPECIAL RECIPES

Prosciutto

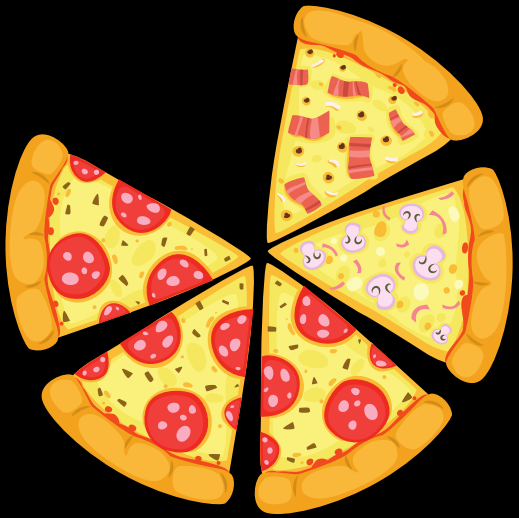
Funghi



Diavolo



Diavolo



Diavolo

Diavolo


»A table for 6 please«

Speculative Cooking


»A table for 6 please«


PIZZA
SPECIAL RECIPES


PIZZA
SPECIAL RECIPES

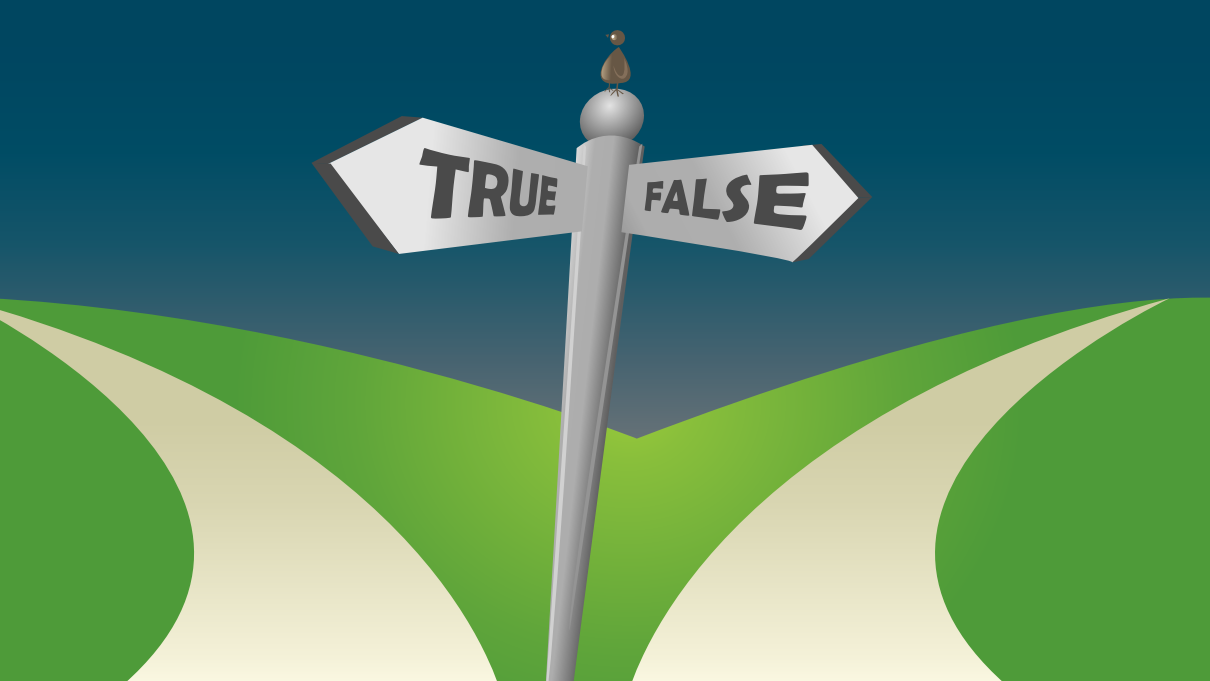

Pizza


PIZZA
SPECIAL RECIPES


Pizza


PIZZA
SPECIAL RECIPES


Pizza


TRUE
FALSE

```
index = 0;

char* data = "textKEY";

if (index < 4)
```


```
LUT[data[index] * 4096]
```

0

```
index = 0;
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```


```
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```

0

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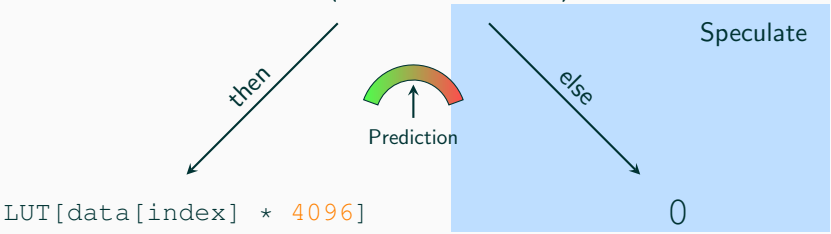

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if (index < 4)
```

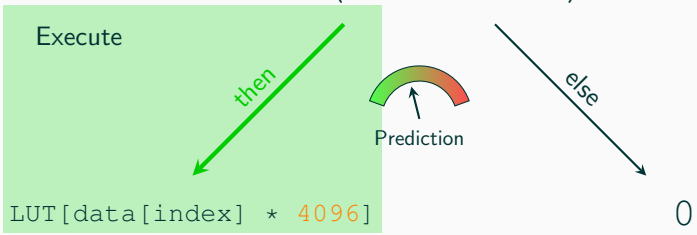

```
index = 1;

char* data = "textKEY";

if (index < 4)
```


```
LUT[data[index] * 4096]
```

0

```
index = 1;
```

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if (index < 4)
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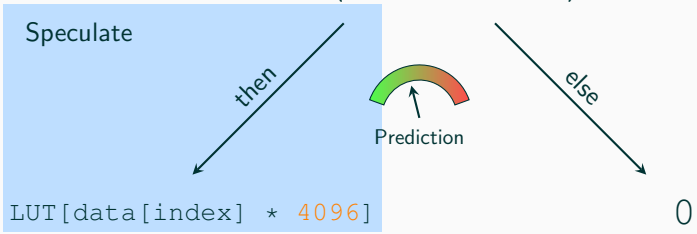

```
index = 1;
```

```
char* data = "textKEY";
```

```
if (index < 4)
```


```
LUT[data[index] * 4096]
```

0

```
index = 2;

char* data = "textKEY";

if (index < 4)
```


```
LUT[data[index] * 4096]
```

0

```
index = 2;
```

```
char* data = "textKEY";
```

```
if (index < 4)
```


```
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```

0

```
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```
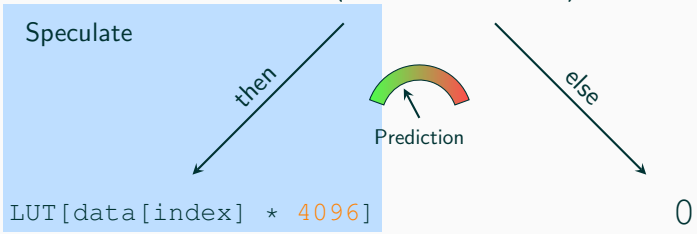

```
char* data = "textKEY";
```

```
if (index < 4)
```



```
index = 2;

char* data = "textKEY";

if (index < 4)
```


```
LUT[data[index] * 4096]
```

0

```
index = 3;

char* data = "textKEY";

if (index < 4)
```


```
LUT[data[index] * 4096]
```

0

```
index = 3;
```

```
char* data = "textKEY";
```

```
if (index < 4)
```

Spectre (variant 1)

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```

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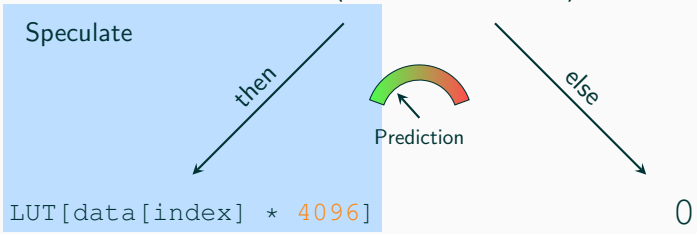

```
index = 3;
```

```
char* data = "textKEY";
```

```
if (index < 4)
```

```
index = 4;

char* data = "textKEY";

if (index < 4)
```


```
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```

0

Spectre (variant 1)

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index = 4;
```

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char* data = "textKEY";
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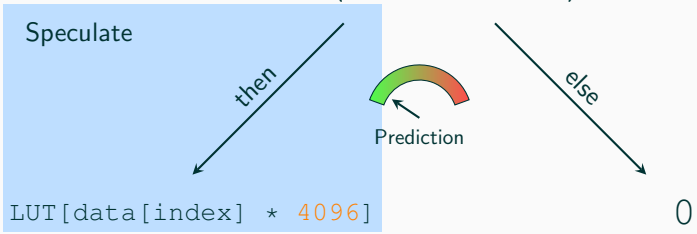
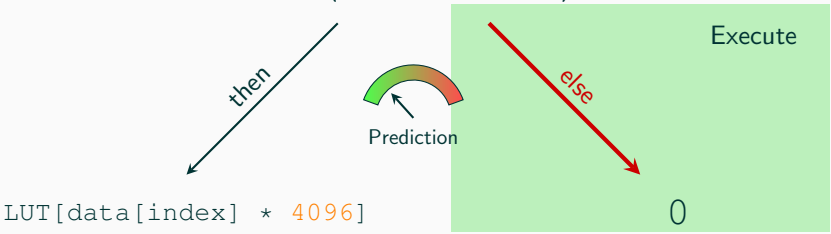


```
index = 4;
```

```
char* data = "textKEY";
```

```
if (index < 4)
```



```
index = 5;

char* data = "textKEY";

if (index < 4)
```


```
LUT[data[index] * 4096]
```

0

```
index = 5;
```

```
char* data = "textKEY";
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```
if (index < 4)
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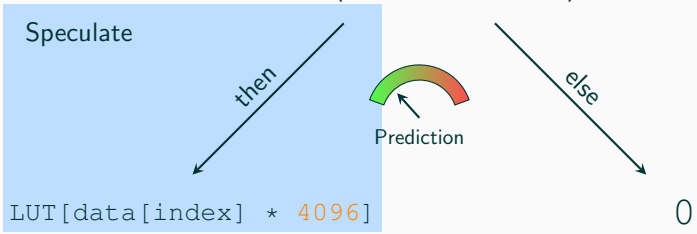

```
index = 5;
```

```
char* data = "textKEY";
```

```
if (index < 4)
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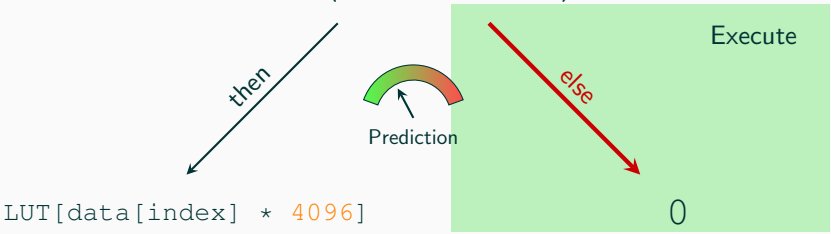

```
index = 6;

char* data = "textKEY";

if (index < 4)
```


```
LUT[data[index] * 4096]
```

0

```
index = 6;
```

```
char* data = "textKEY";
```

```
if (index < 4)
```


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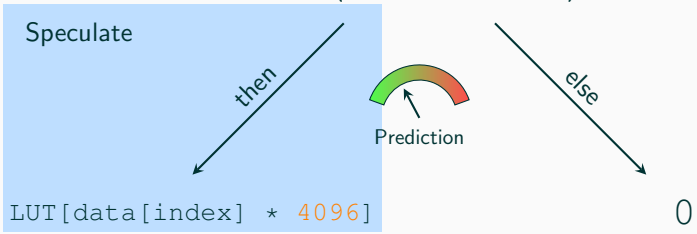

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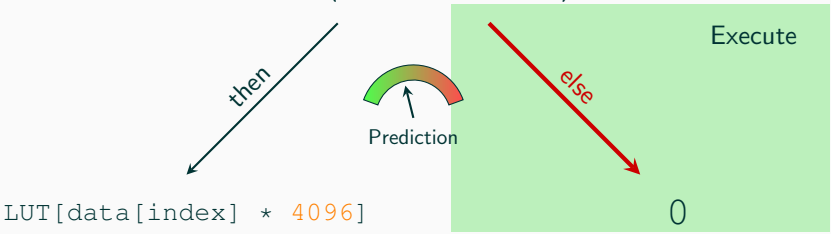
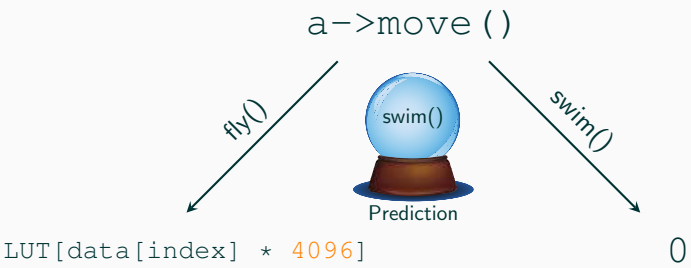


```
Animal* a = bird;
```



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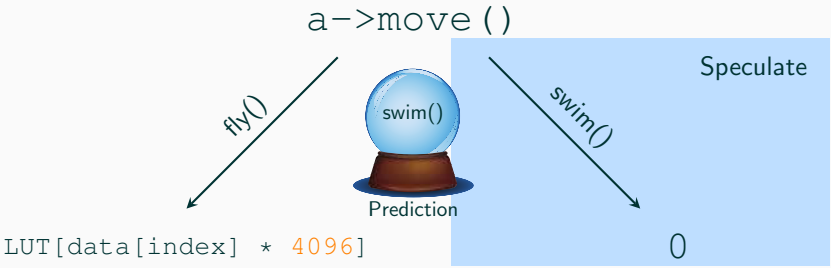

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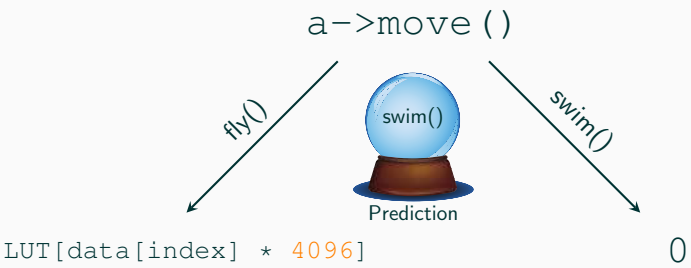

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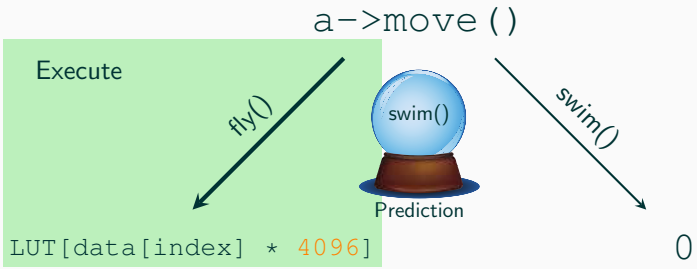

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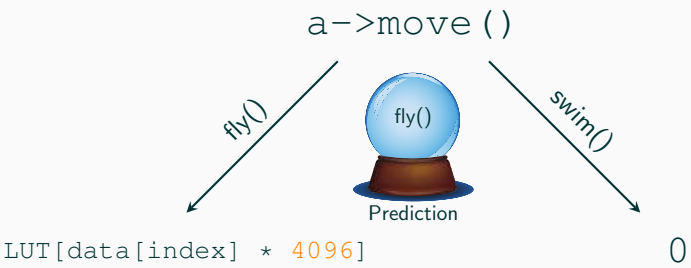

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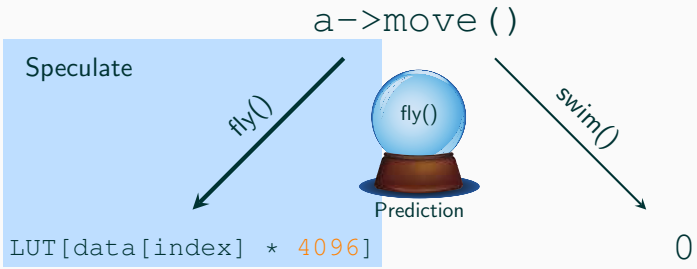

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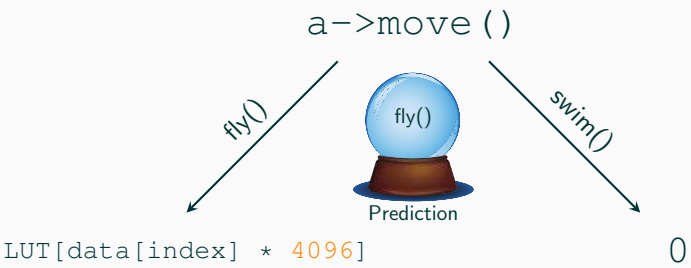

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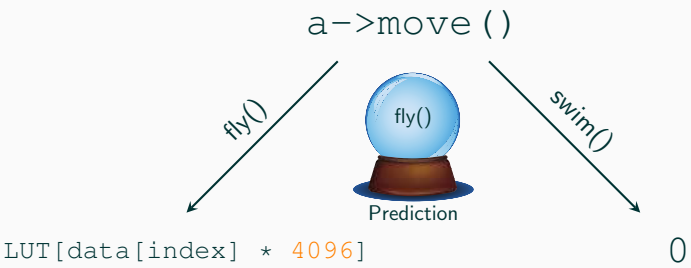

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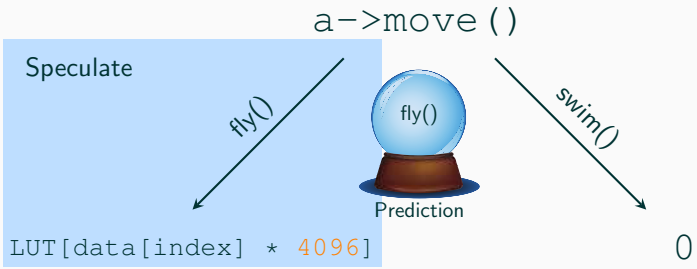

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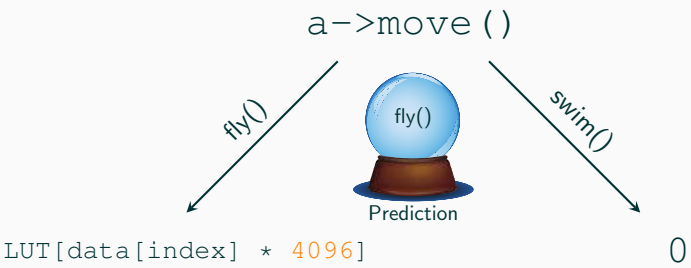

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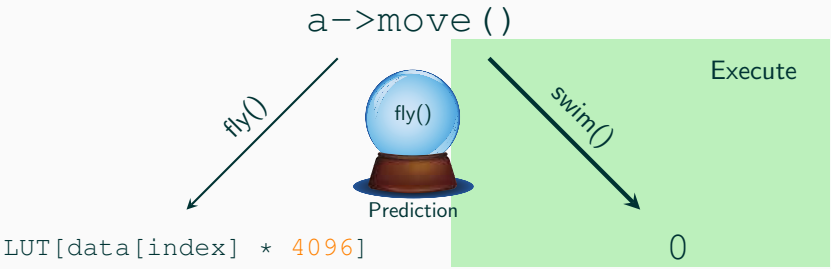

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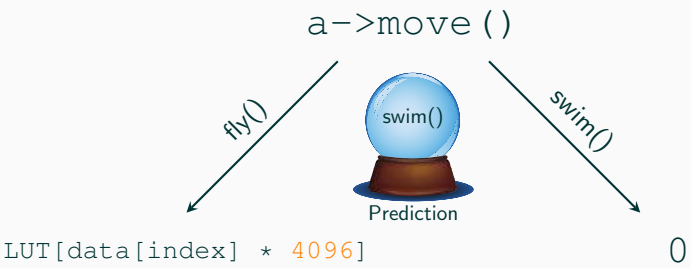

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Spectre

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- Much harder to fix, KAISER does not help
- Ongoing effort to patch via microcode update and compiler extensions

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- No wrong speculation if there is no speculation
- Problem: massive performance hit!
- Also: How to disable it?
- Speculative execution is deeply integrated into CPU


GHOSTBUSTERS

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$\rightarrow$ insert after every bounds check

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- x86: `LFENCE`, ARM: `CSDB`

Spectre Variant 1 Mitigations

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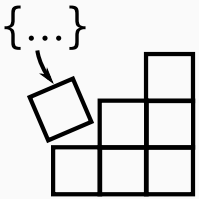
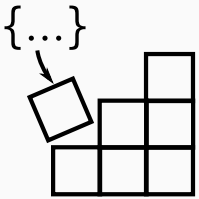
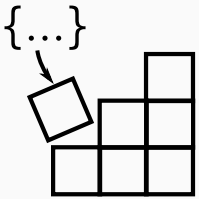
→ insert after every bounds check

- x86: `LFENCE`, ARM: `CSDB`
- Available on all Intel CPUs, retrofitted to existing ARMv7 and ARMv8





- Speculation barrier requires compiler supported



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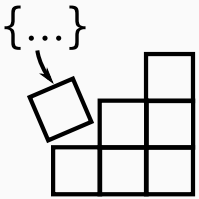

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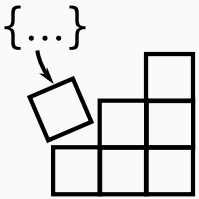
Spectre Variant 1 Mitigations



- Speculation barrier requires compiler supported
- Already implemented in GCC, LLVM, and MSVC
- Can be automated (MSVC) → not really reliable
- Explicit use by programmer: `__builtin_load_no_speculate`

Spectre Variant 1 Mitigations

```
// Unprotected

int array[N];

int get_value(unsigned int n) {
  int tmp;

  if (n < N) {
    tmp = array[n]
  } else {
    tmp = FAIL;
  }

  return tmp;
}
```

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int array[N];

int get_value(unsigned int n) {
  int tmp;

  if (n < N) {
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  } else {
    tmp = FAIL;
  }

  return tmp;
}
```

```
// Protected

int array[N];

int get_value(unsigned int n) {

  int *lower = array;
  int *ptr = array + n;
  int *upper = array + N;

  return
    __builtin_load_no_speculate
    (ptr, lower, upper, FAIL);

}
```


GHOSTBUSTERS

- Speculation barrier works if affected code constructs are known

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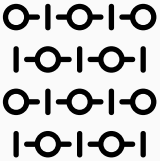
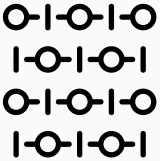
- Non-negligible performance overhead of barriers



Intel released microcode updates

- Indirect Branch Restricted Speculation (IBRS):



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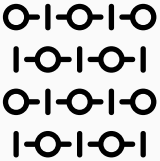

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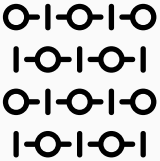

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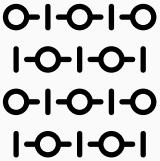

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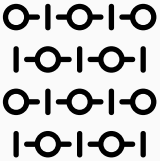

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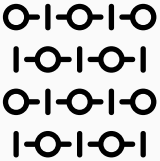

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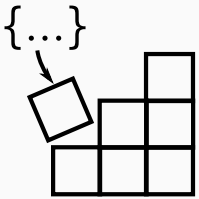
Retpoline (compiler extension)



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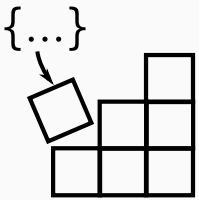


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    push <call_target>
    call 1f
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    lfence              ; speculation barrier
    jmp 2b              ; endless loop
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    lea 8(%rsp), %rsp   ; restore stack pointer
    ret                 ; the actual call to <call_target>
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→ always predict to enter an endless loop

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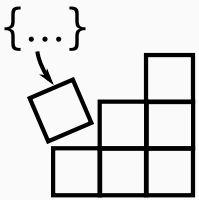


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→ always predict to enter an endless loop

- instead of the correct (or wrong) target function

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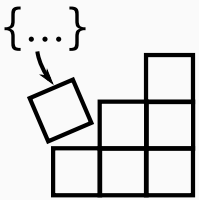


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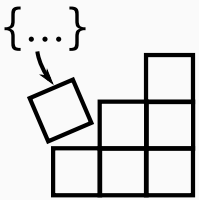
Retpoline (compiler extension)



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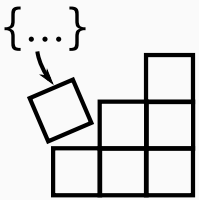

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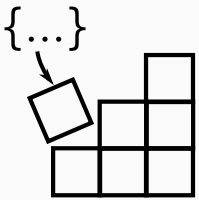


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  → microcode patches to prevent that

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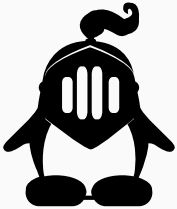

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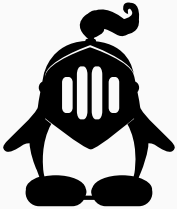

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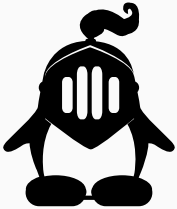

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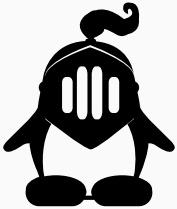

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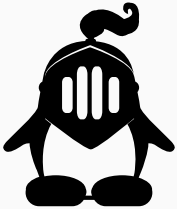

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- Clears branch-predictor state on context switch
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- Non-negligible performance overhead ($\approx$ 200-300 ns)

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→ Spectre works on secure enclaves

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→ for years we solely optimized for performance

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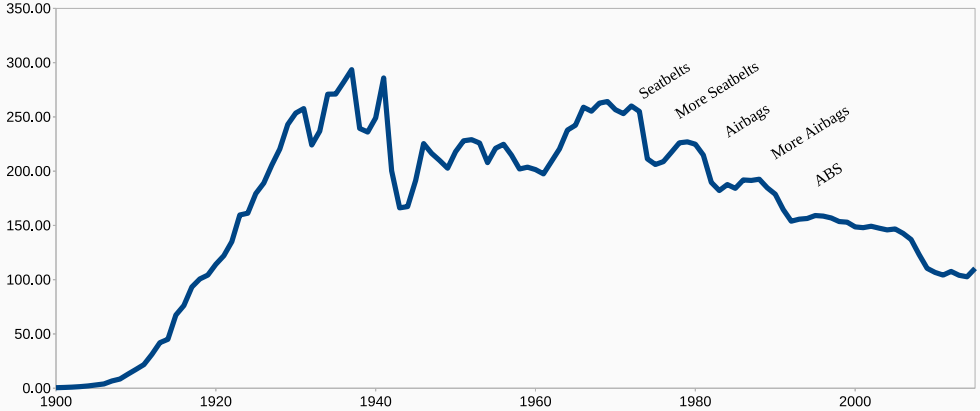


Motor Vehicle Deaths in U.S. by Year

A unique chance

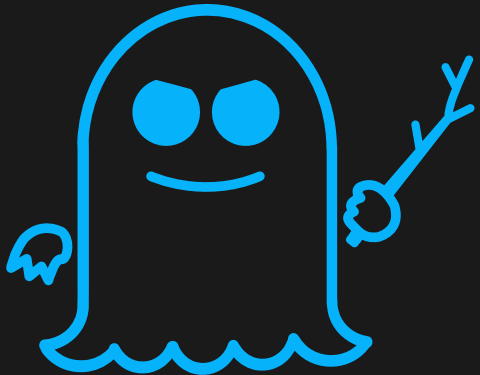
A unique chance to

- rethink processor design
- grow up, like other fields (car industry, construction industry)
- find good trade-offs between security and performance

Conclusion

- Underestimated microarchitectural attacks for a long time
  - Basic techniques were there for years
- Industry and customers must embrace security mechanisms
  - Run through the same development (for security) as the automobile industry (for safety)
  - It should not be “performance first”, but “security first”

MELTDOWN



SPECTRE


FACt
MELTDOWN
SPECTRE

Any Questions?

Factor:
Das Unfassbare

Die Geschichte von
Meltdown und Spectre

Michael Schwarz
(@misc0110)