Spectre and Meltdown on x86 and ARM

Michael Schwarz, Moritz Lipp, Stefan Mangard

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Vulnerability Assessment

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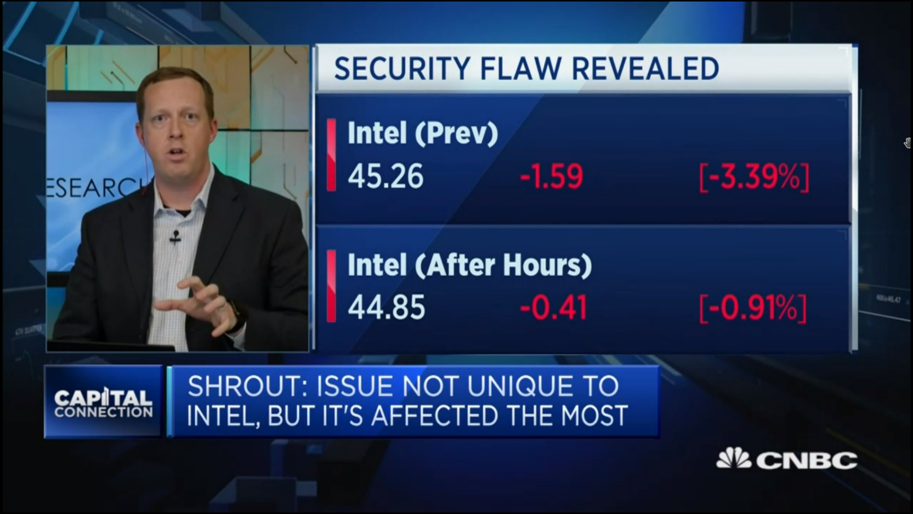
- Meltdown and Spectre are two CPU vulnerabilities
- Discovered in 2017 by 4 independent teams
- Due to an embargo, released at the beginning of 2018
- News coverage followed by a lot of panic

FOX BUSINESS WASHINGTON, D.C.
WASHINGTON, D.C.
WINTER STORM
NEWS ALERT
INTEL REVEALS DESIGN FLAW THAT COULD ALLOW HACKERS TO ACCESS DATA
FOX BUSINESS NETWORK
@FOXBUSINESS

FIREEYE CYBER THREAT MAP
DEVELOPING STORY
COMPUTER CHIP FLAWS IMPACT BILLIONS OF DEVICES
LIVE
CNN
DAX ▲164.69
NEWS STREAM

GLOBAL
COMPUTER CHIP SCARE
The bugs are known as 'Spectre' and 'Meltdown'
BBC WORLD NEWS
£:HKS 10.58
EURO:£ 0.891



SECURITY FLAW REVEALED

Intel (Prev)		
45.26	-1.59	[-3.39%]
Intel (After Hours)		
44.85	-0.41	[-0.91%]

CAPITAL CONNECTION

SHROUT: ISSUE NOT UNIQUE TO INTEL, BUT IT'S AFFECTED THE MOST

Vulnerability Assesment

A lot of confusion fueled the panic

- Which CPUs/vendors are affected?

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- What data is at risk?
- How hard is it to exploit the vulnerabilities?

Vulnerability Assesment

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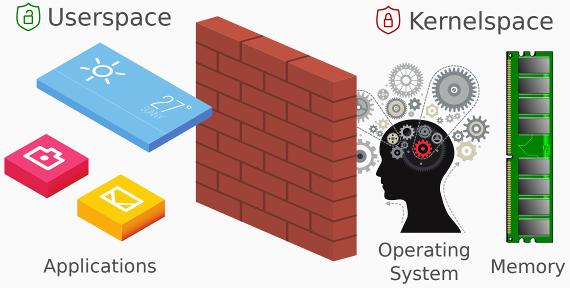
- Which CPUs/vendors are affected?
- Are smartphones/IoT devices affected?
- Can the vulnerabilities be exploited remotely?
- What data is at risk?
- How hard is it to exploit the vulnerabilities?
- Is it already exploited?

Let’s try to clarify these questions

MELTDOWN

Hardware Isolation

- Kernel is isolated from user space



Hardware Isolation

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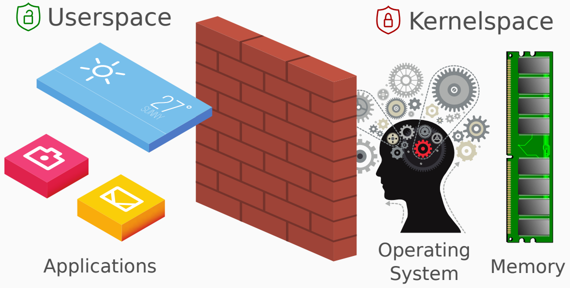

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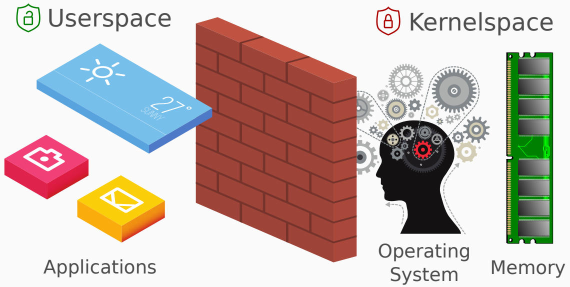

Hardware Isolation

- Kernel is isolated from user space
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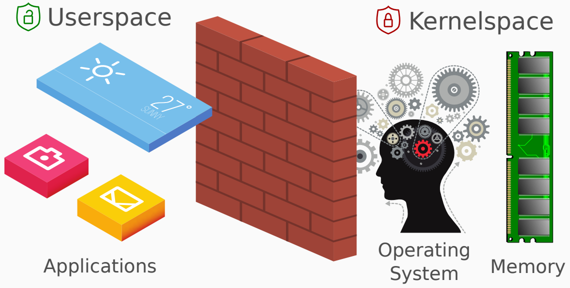
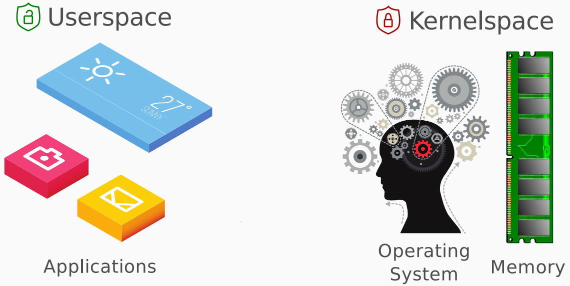
- User applications cannot access anything from the kernel
- There is only a well-defined interface → syscalls



Meltdown Briefing

- Breaks isolation between applications and kernel



Meltdown Briefing

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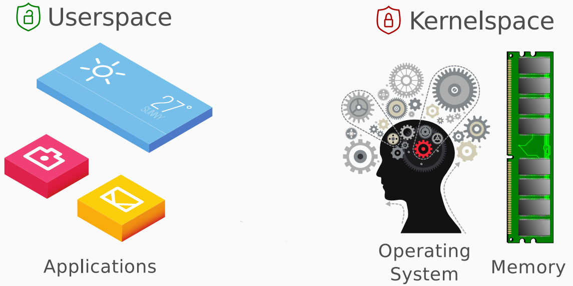

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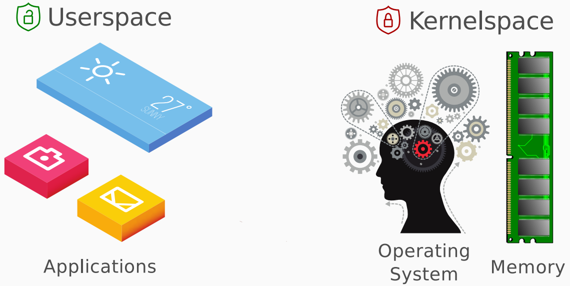

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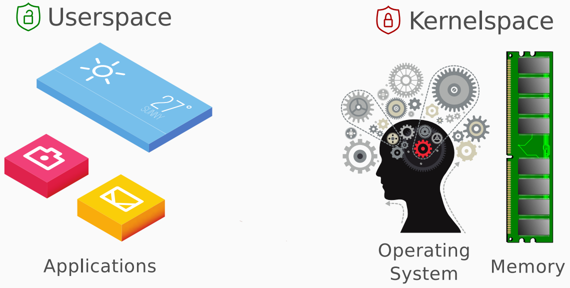
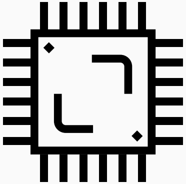
→ Meltdown can read whole DRAM



Meltdown Requirements

- Only on Intel CPUs and some unreleased ARMs (Cortex A75)

Meltdown Requirements



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- Common cause: permission check done in parallel to load instruction
- Race condition between permission check and dependent operation(s)

Meltdown Variant Requirements

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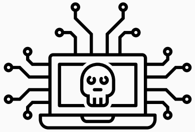
- Limited to some registers, no memory content
- Reported by ARM
- Affects some ARMs (Cortex A15, A57, and A72)

Meltdown Exploitability



- Meltdown requires code execution on the device (e.g. Apps)

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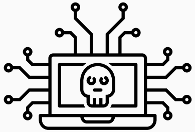

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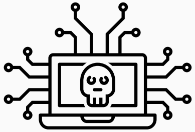
- Untrusted code can read entire memory of device

Meltdown Exploitability



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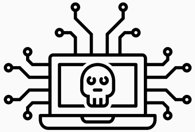

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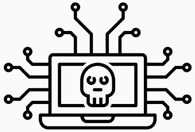

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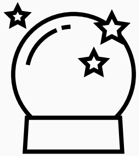
- No info about environment required → easy to reproduce

SPECTRE

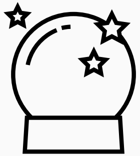
Spectre Briefing

- Mistrains branch prediction



Spectre Briefing

- Mistrains branch prediction
- CPU speculatively executes code which should not be executed



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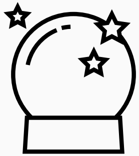
$\rightarrow$ Spectre "convinces" program to execute code



Spectre Requirements

- On Intel and AMD CPUs

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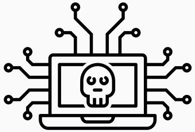
- Some ARMs (Cortex R and Cortex A) are also affected
- Common cause: speculative execution of branches
- Speculative execution leaves microarchitectural traces which leak secret

Spectre Exploitability



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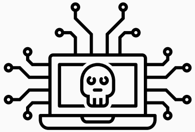

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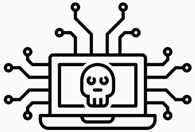

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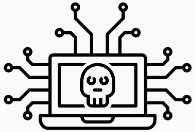

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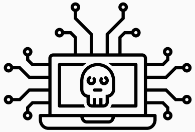

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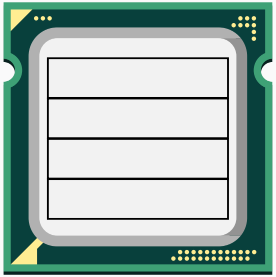
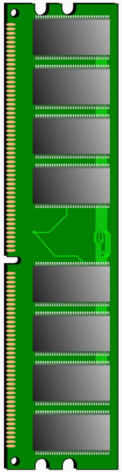
Background

CPU Cache

```
printf("%d", i);
printf("%d", i);
```





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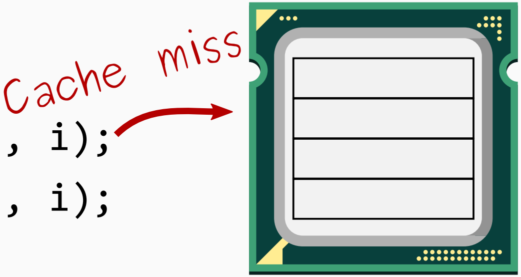

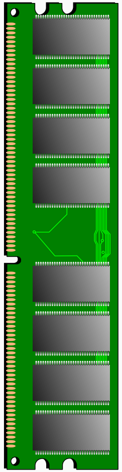

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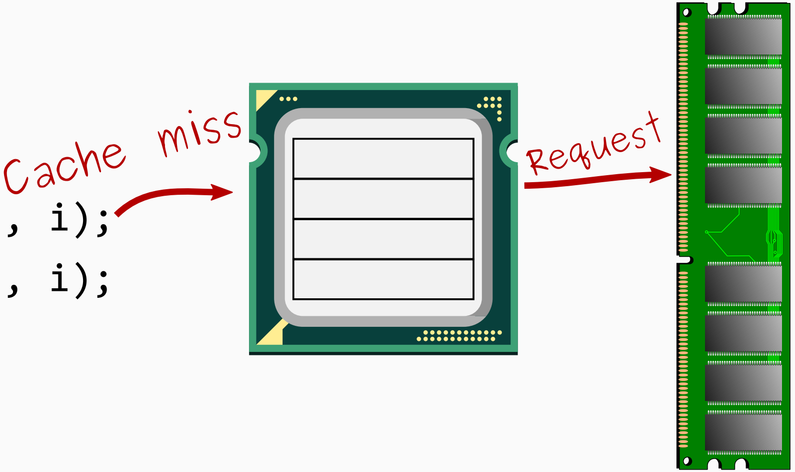

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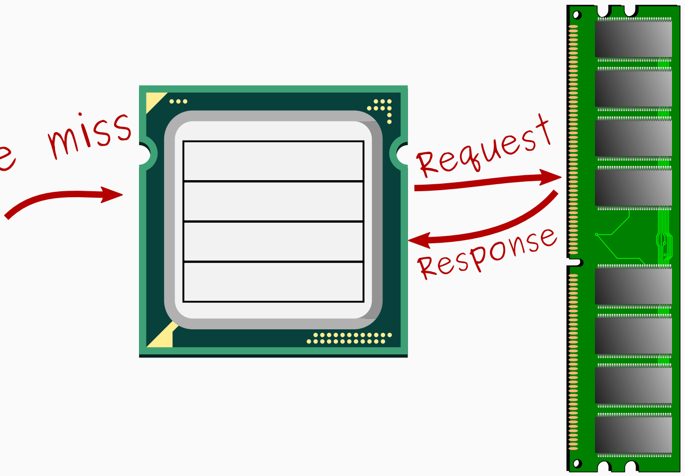

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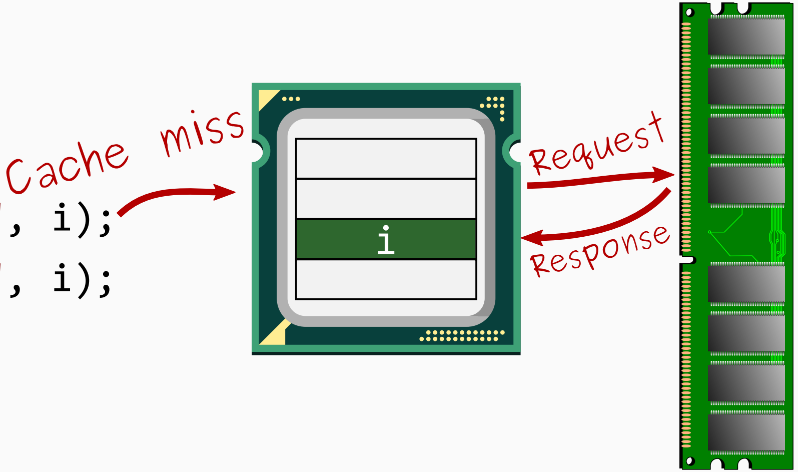

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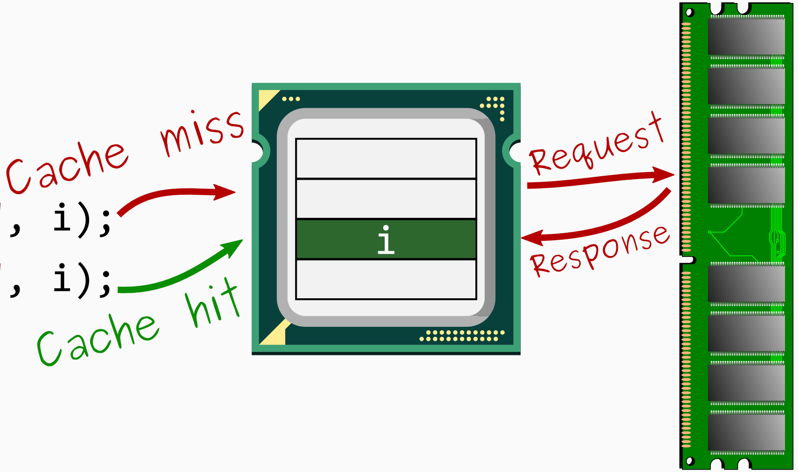

CPU Cache

DRAM access, slow

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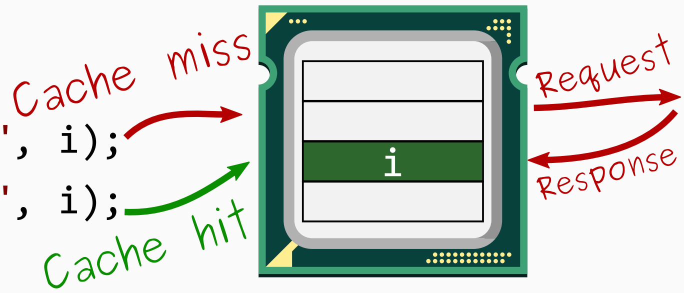

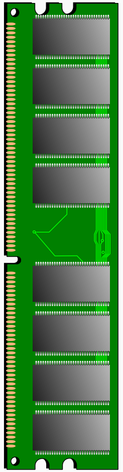

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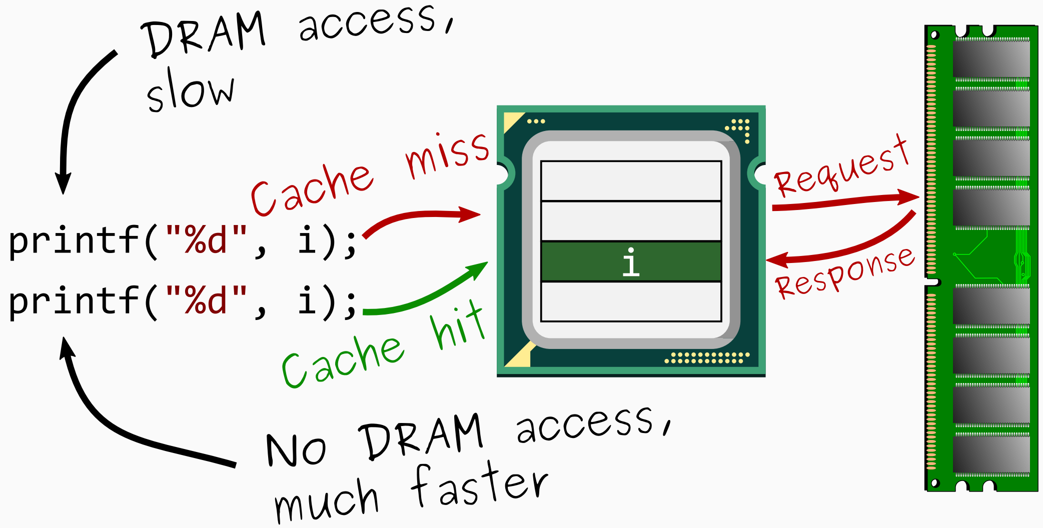

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Flush+Reload

Shared Memory

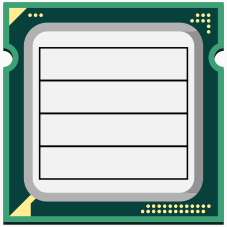
ATTACKER

flush

access

VICTIM

access



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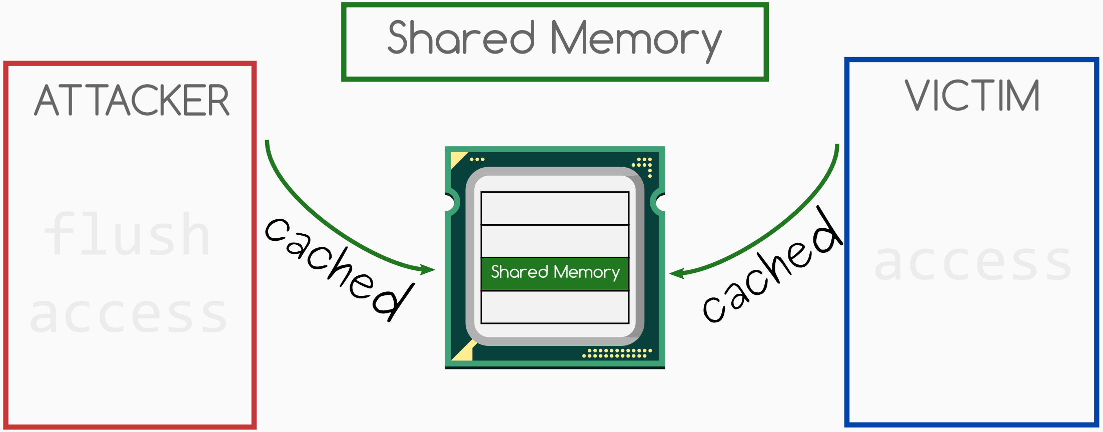

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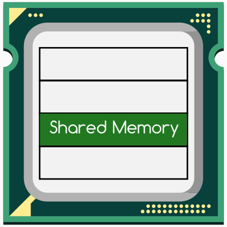

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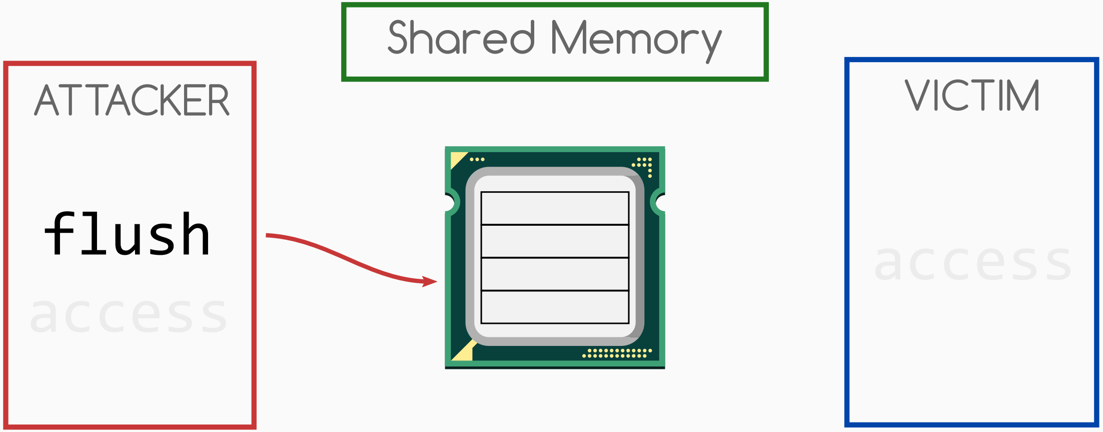

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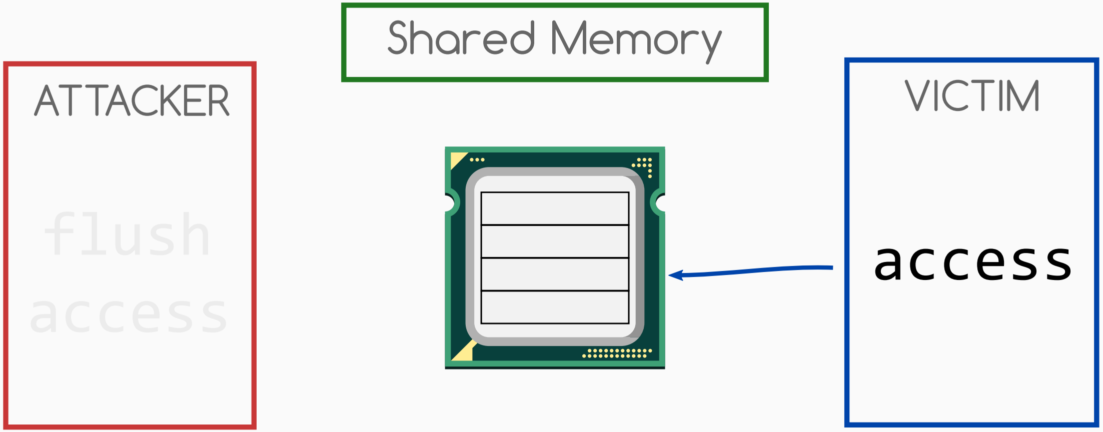

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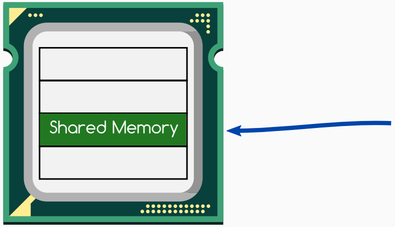

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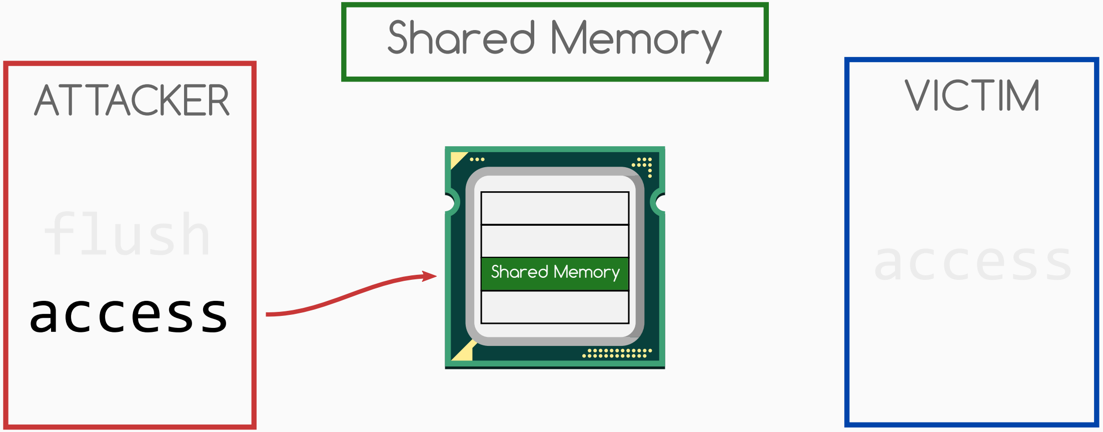

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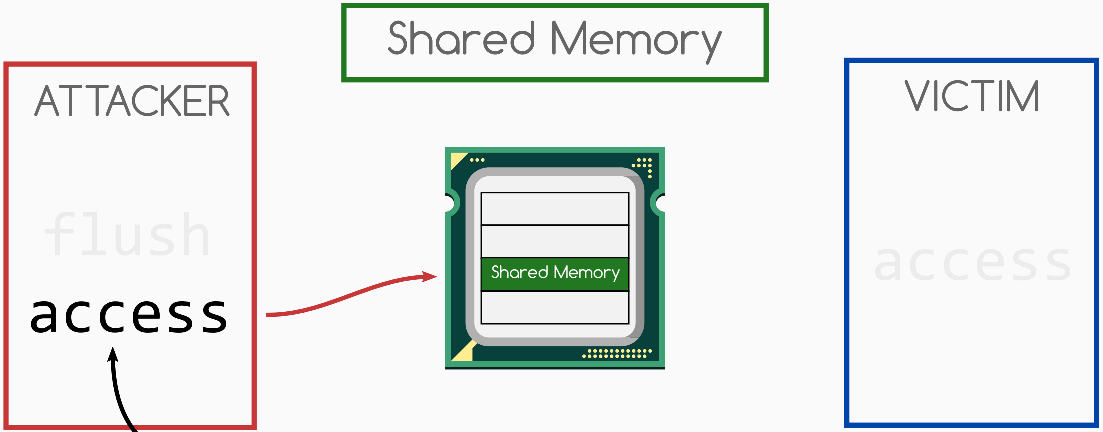


fast if victim accessed data,
slow otherwise

Out-of-order Execution

5. Cook everything until vegetables are soft

6. Add spices to taste [illegible] for 10 minutes

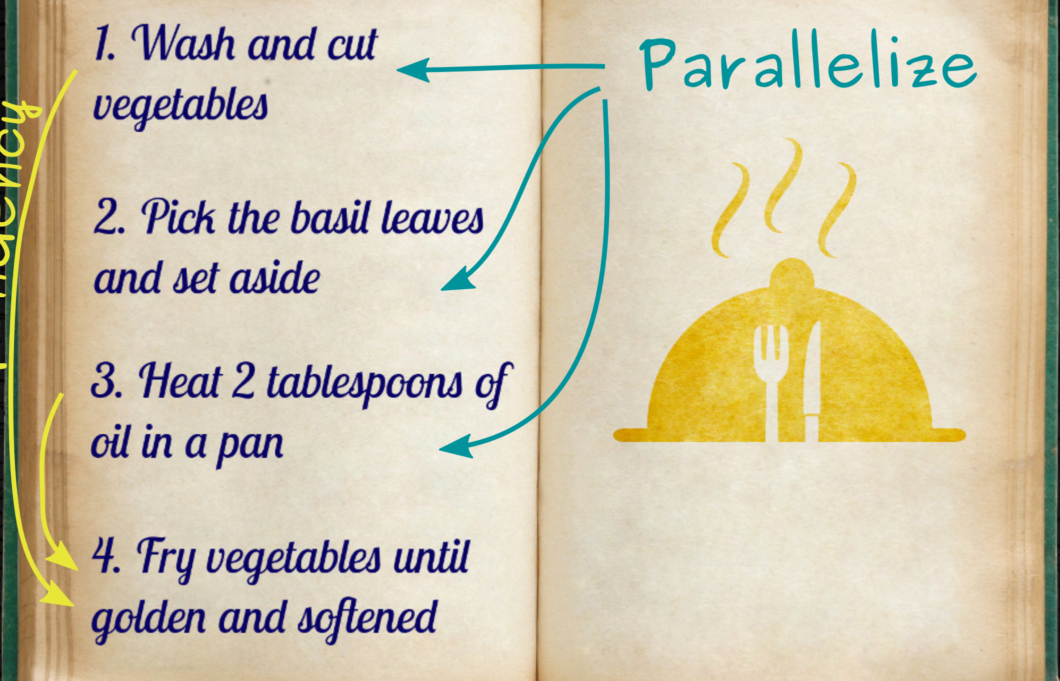
7. Serve with cooked and peeled potatoes

Wait for an hour

Wait for an hour

LATENCY

1. Wash and cut vegetables
2. Pick the basil leaves and set aside
3. Heat 2 tablespoons of oil in a pan
4. Fry vegetables until golden and softened



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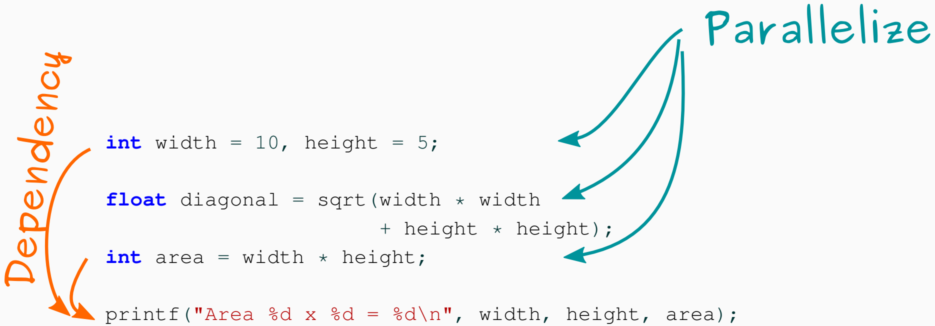
Out-of-order Execution

```
int width = 10, height = 5;

float diagonal = sqrt(width * width
                      + height * height);
int area = width * height;

printf("Area %d x %d = %d\n", width, height, area);
```

Out-of-order Execution



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We are ready for the gory details of Meltdown

Building Meltdown

```
char data = *(char*)0xffffffff81a000e0;
printf("%c\n", data);
```

Building Meltdown

```c
char data = *(char*)0xffffffff81a000e0;
printf("%c\n", data);
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```
segfault at ffffffff81a000e0 ip 0000000000400535
            sp 00007ffce4a80610 error 5 in reader
```

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- Kernel addresses are not accessible

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segfault at ffffffff81a000e0 ip 0000000000400535
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```

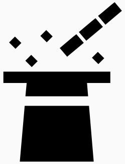
- Kernel addresses are not accessible
- Are privilege checks also done when executing instructions out of order?

Building Meltdown

- Adapted code

```
*(volatile char*)0;
array[84 * 4096] = 0; // unreachable
```

Building Meltdown



- Adapted code

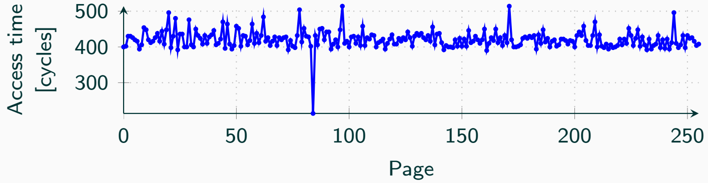
```
*(volatile char*)0;
array[84 * 4096] = 0; // unreachable
```

- Static code analyzer is not happy

```
warning: Dereference of null pointer
         *(volatile char*)0;
```

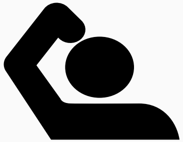
Building Meltdown

- Flush+Reload over all pages of the array

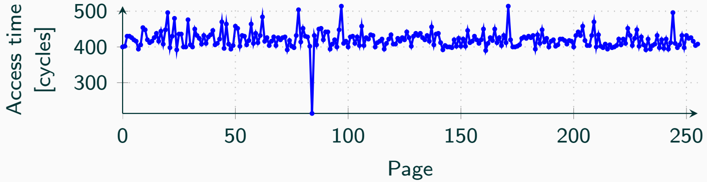


- “Unreachable” code line was actually executed

Building Meltdown



- Flush+Reload over all pages of the array



- “Unreachable” code line was actually executed
- Exception was only thrown afterwards

Building Meltdown

- Out-of-order instructions leave microarchitectural traces

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- Give such instructions a name: transient instructions

Building Meltdown

- Out-of-order instructions leave microarchitectural traces
- We can see them for example in the cache
- Give such instructions a name: transient instructions
- We can indirectly observe the execution of transient instructions

Building Meltdown

- Combine the two things

```
char data = *(char*)0xffffffff81a000e0;
array[data * 4096] = 0;
```

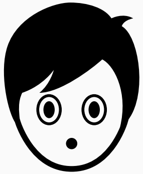
Building Meltdown

- Combine the two things

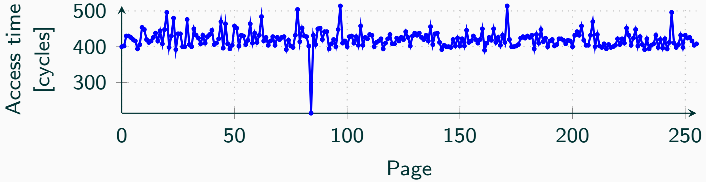
```
char data = *(char*)0xffffffff81a000e0;
array[data * 4096] = 0;
```

- Then check whether any part of `array` is cached

Building Meltdown

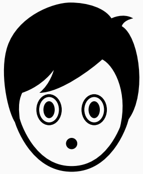


- Flush+Reload over all pages of the array

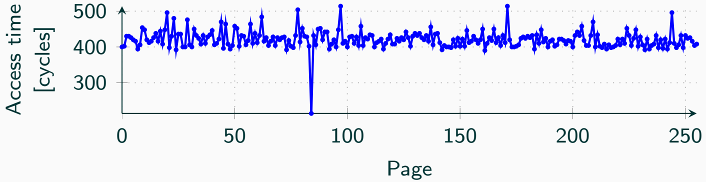


- Index of cache hit reveals data

Building Meltdown

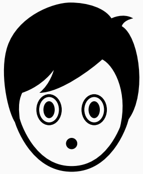


- Flush+Reload over all pages of the array



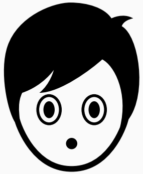
- Index of cache hit reveals data
- Permission check is in some cases not fast enough

Building Meltdown



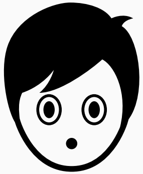
- Using out-of-order execution, we can read data at any address

Building Meltdown



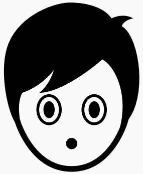
- Using out-of-order execution, we can read data at any address
- Privilege checks are sometimes too slow

Building Meltdown

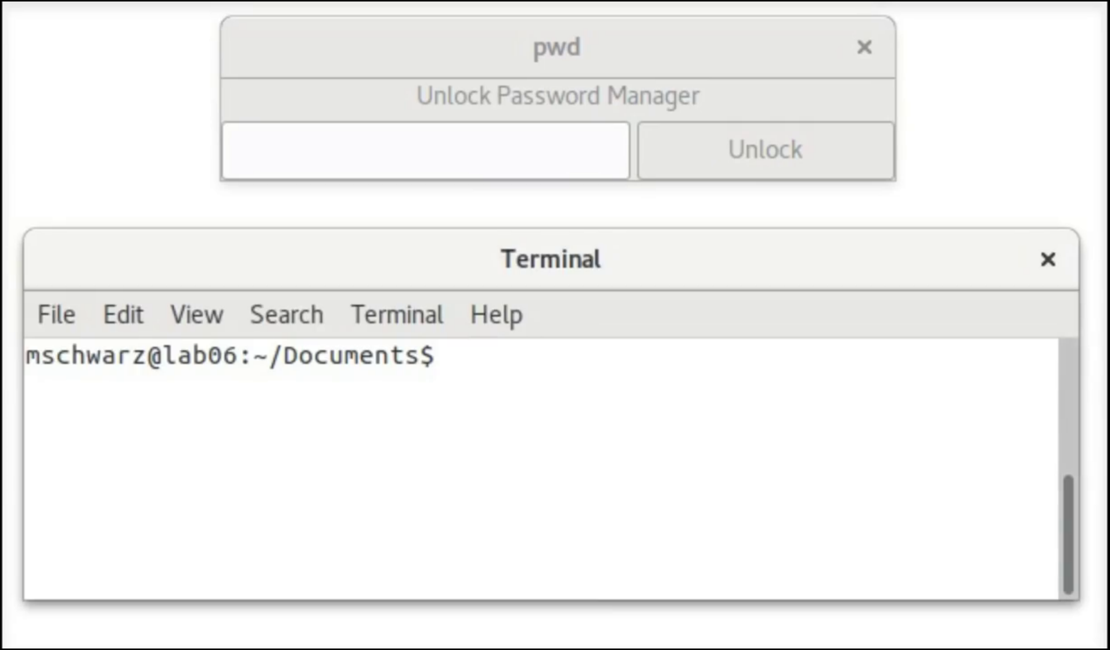


- Using out-of-order execution, we can read data at any address
- Privilege checks are sometimes too slow
- Allows to leak kernel memory

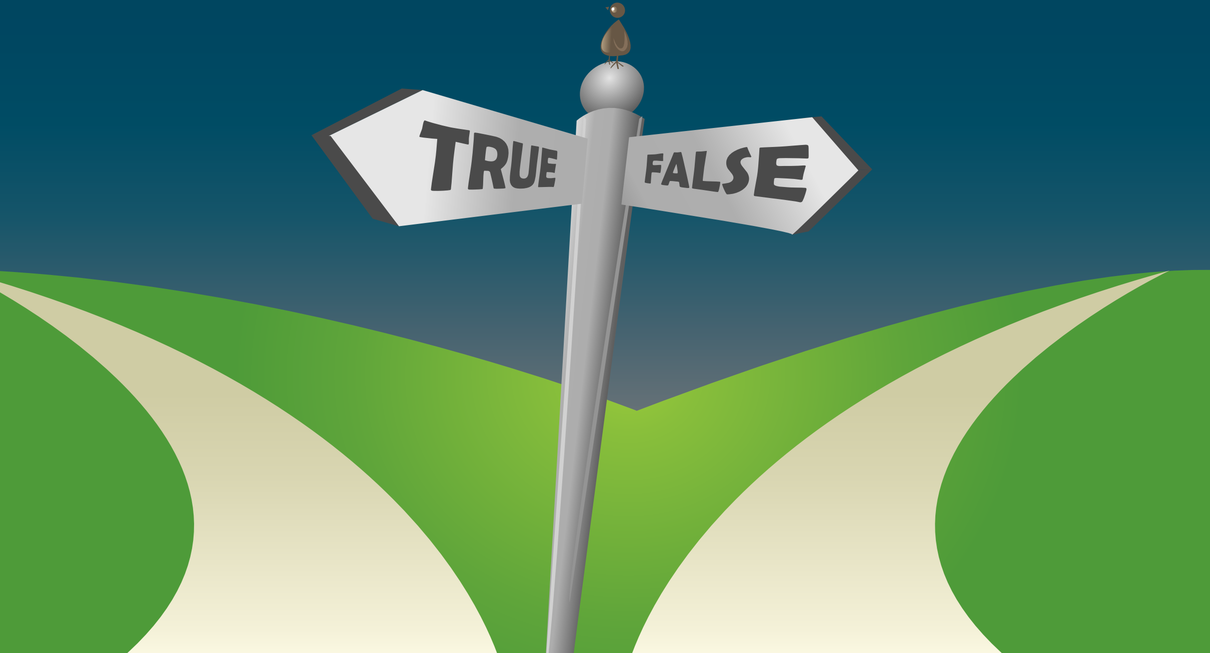
Building Meltdown



- Using out-of-order execution, we can read data at any address
- Privilege checks are sometimes too slow
- Allows to leak kernel memory
- Entire physical memory is typically also accessible in kernel address space



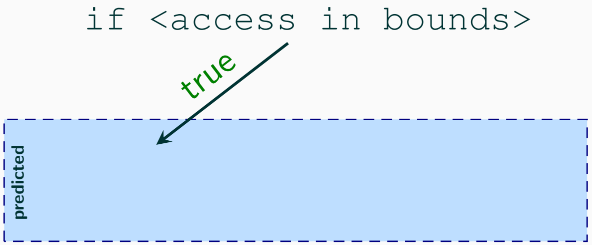
```
mschwarz@lab06:~/Documents$
```


TRUE
FALSE

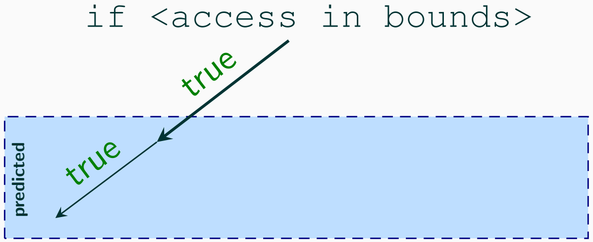
Spectre

```
if <access in bounds>
```

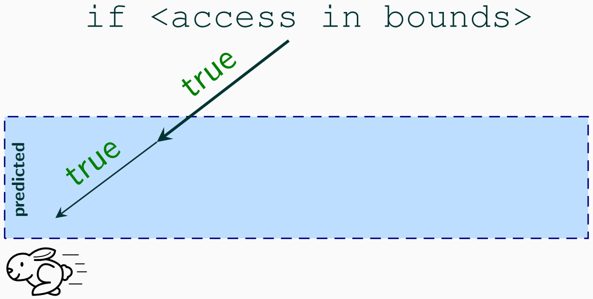
Spectre



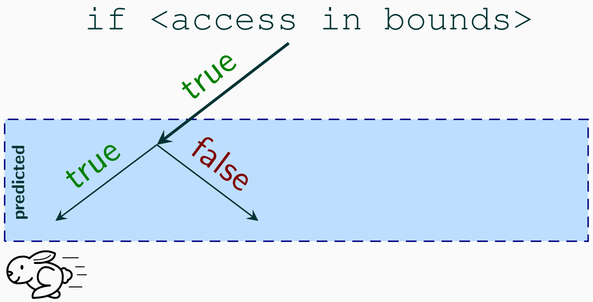
Spectre



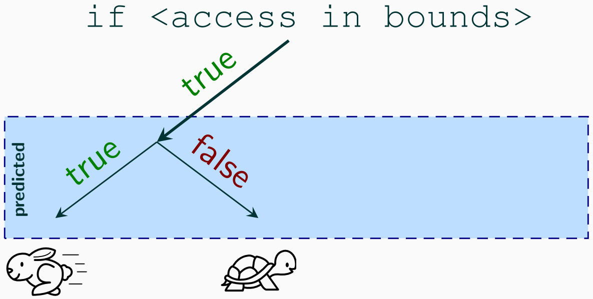
Spectre



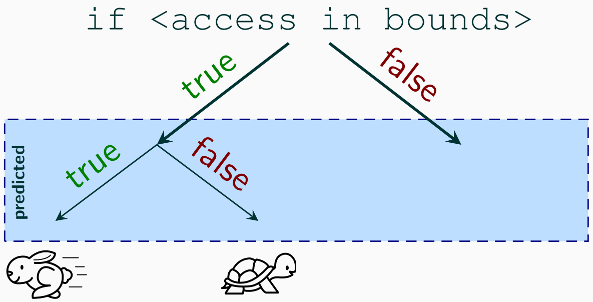
Spectre



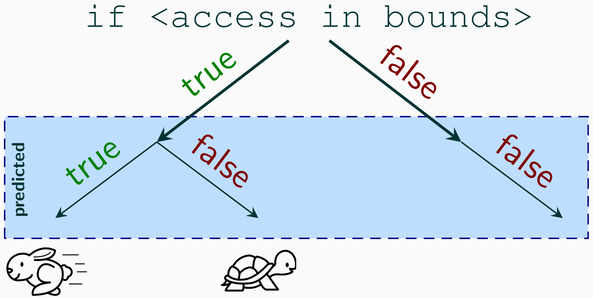
Spectre



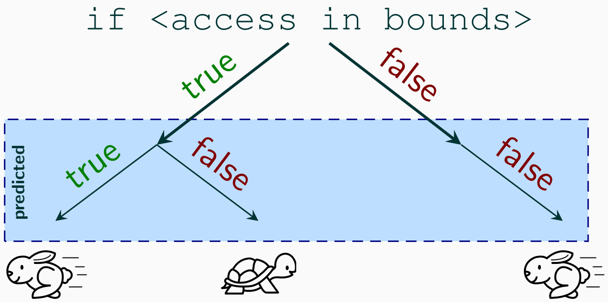
Spectre



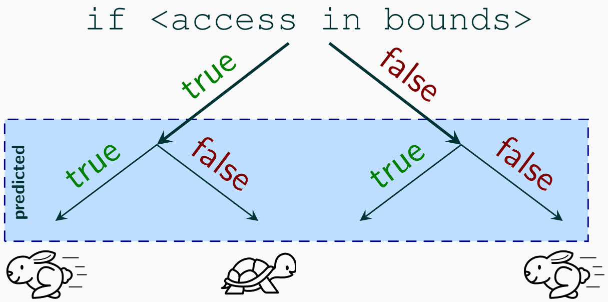
Spectre



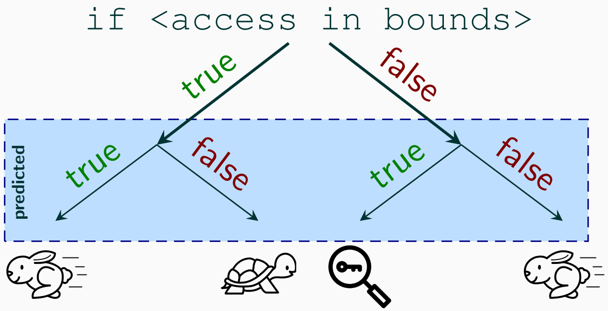
Spectre



Spectre



Spectre



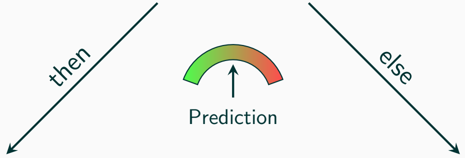
We are ready for the gory details of Spectre

Spectre (variant 1)

```
index = 0;

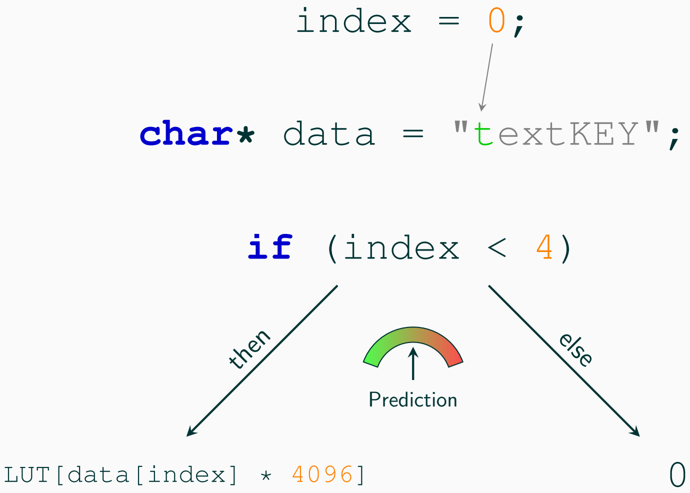
char* data = "textKEY";

if (index < 4)
```



```
LUT[data[index] * 4096]                    0
```

Spectre (variant 1)

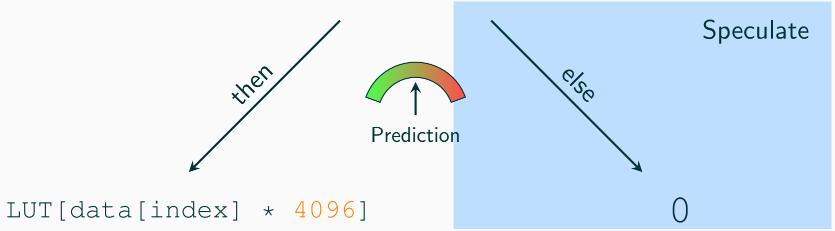


Spectre (variant 1)

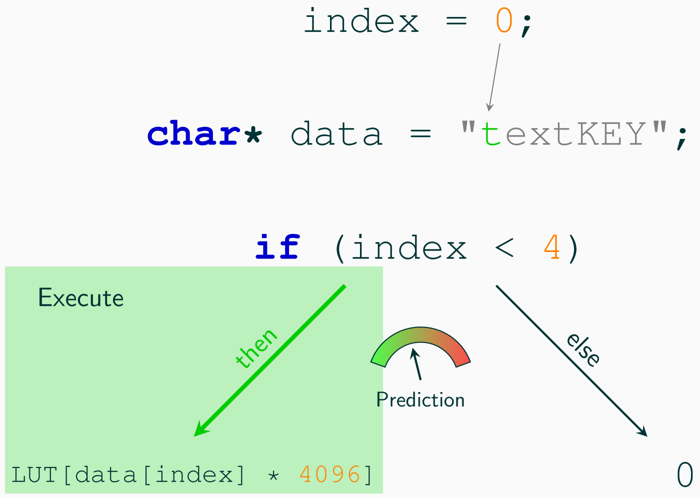
```
index = 0;

char* data = "textKEY";

if (index < 4)
```



Spectre (variant 1)



```
index = 0;

char* data = "textKEY";

if (index < 4)

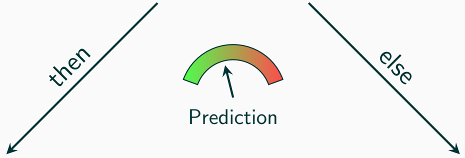
LUT[data[index] * 4096]
```

Spectre (variant 1)

```
index = 1;

char* data = "textKEY";

if (index < 4)
```



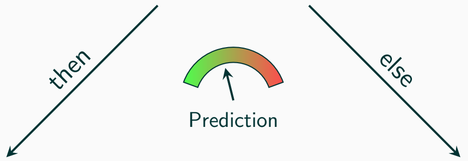
```
LUT[data[index] * 4096]                    0
```

Spectre (variant 1)

```
index = 1;

char* data = "textKEY";

if (index < 4)
```



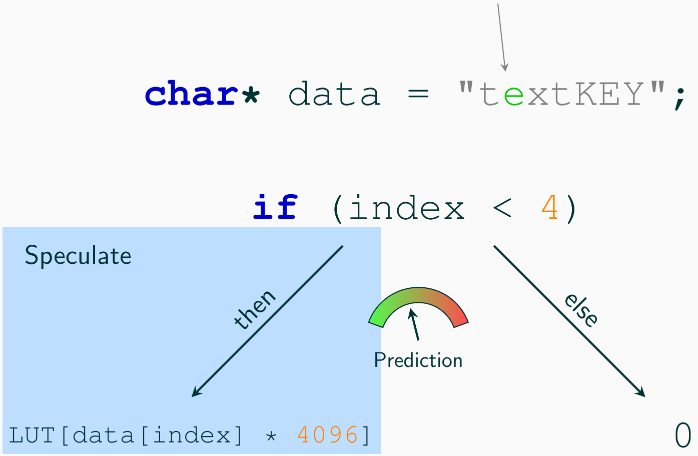
```
LUT[data[index] * 4096]                0
```

Spectre (variant 1)

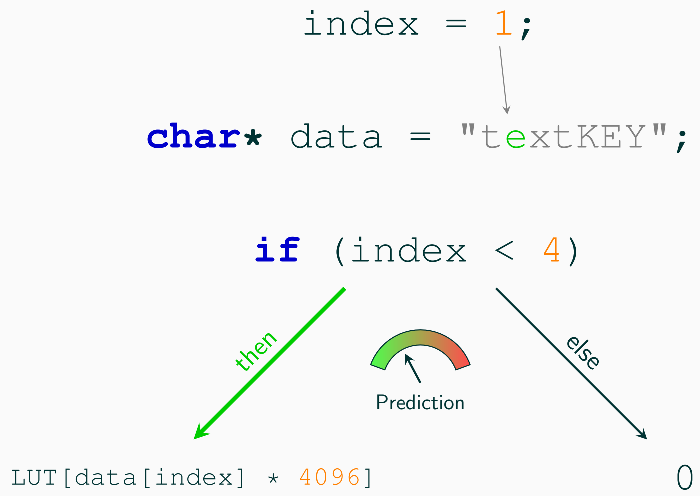
```
index = 1;

char* data = "textKEY";

if (index < 4)
```



Spectre (variant 1)



```
index = 1;

char* data = "textKEY";

if (index < 4)
```

```
LUT[data[index] * 4096]
```

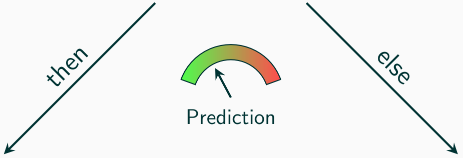
0

Spectre (variant 1)

```
index = 2;

char* data = "textKEY";

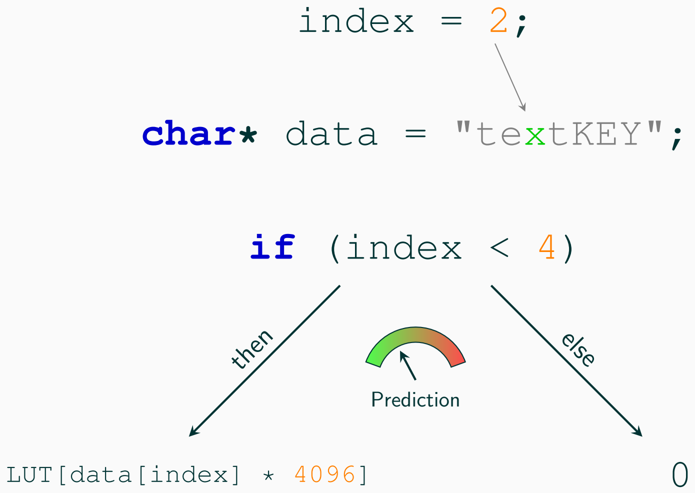
if (index < 4)
```



```
LUT[data[index] * 4096]
```

0

Spectre (variant 1)

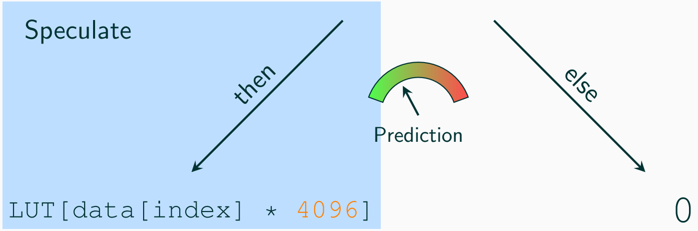


Spectre (variant 1)

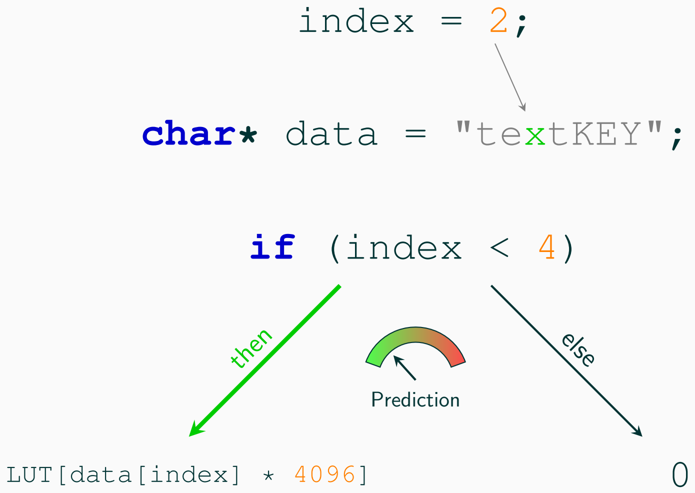
```
index = 2;

char* data = "textKEY";

if (index < 4)
```



Spectre (variant 1)



```
index = 2;

char* data = "textKEY";

if (index < 4)
```

```
LUT[data[index] * 4096]
```

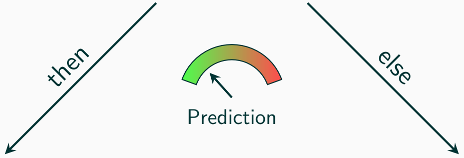
```
0
```

Spectre (variant 1)

```
index = 3;

char* data = "textKEY";

if (index < 4)
```



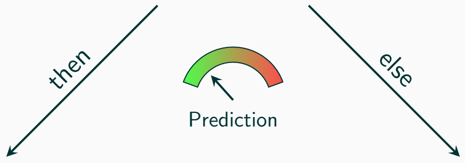
```
LUT[data[index] * 4096]                0
```

Spectre (variant 1)

```
index = 3;

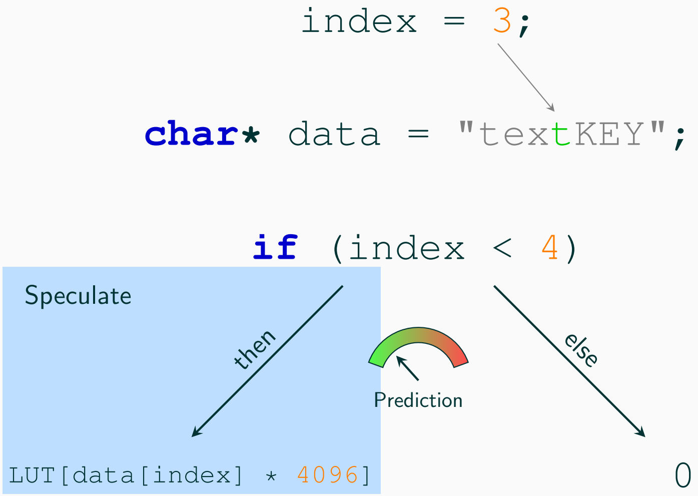
char* data = "textKEY";

if (index < 4)
```

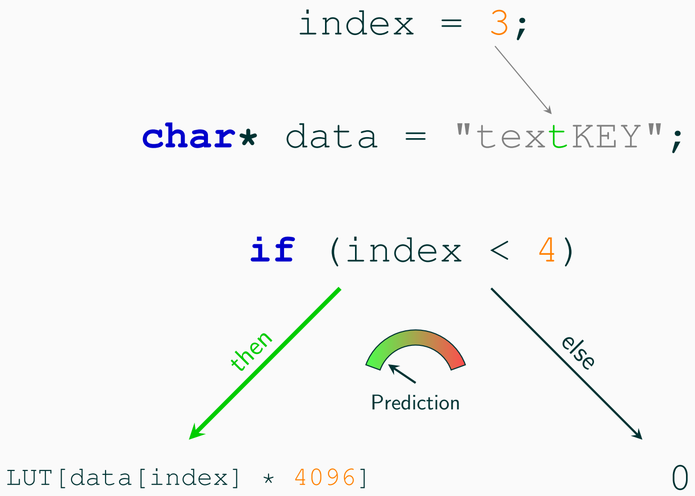


```
LUT[data[index] * 4096]                0
```

Spectre (variant 1)



Spectre (variant 1)



```
index = 3;

char* data = "textKEY";

if (index < 4)

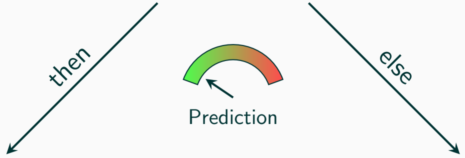
LUT[data[index] * 4096]                    0
```

Spectre (variant 1)

```
index = 4;

char* data = "textKEY";

if (index < 4)
```



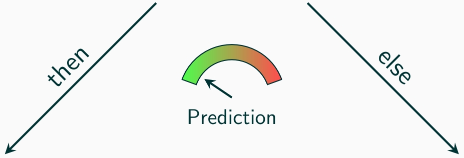
```
LUT[data[index] * 4096]                    0
```

Spectre (variant 1)

```
index = 4;

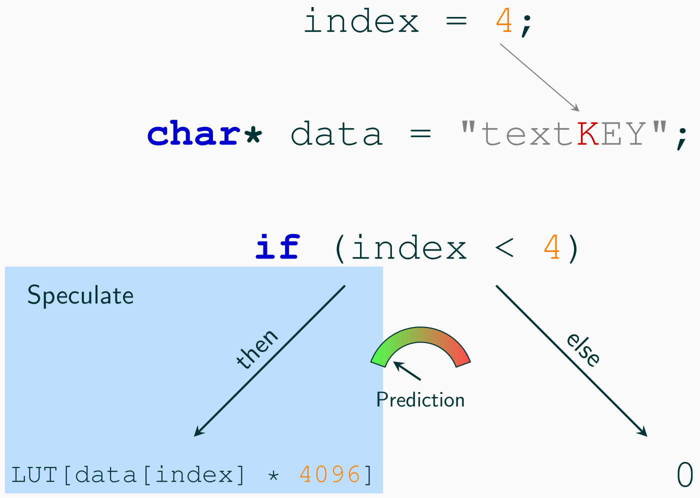
char* data = "textKEY";

if (index < 4)
```



```
LUT[data[index] * 4096]                 0
```

Spectre (variant 1)

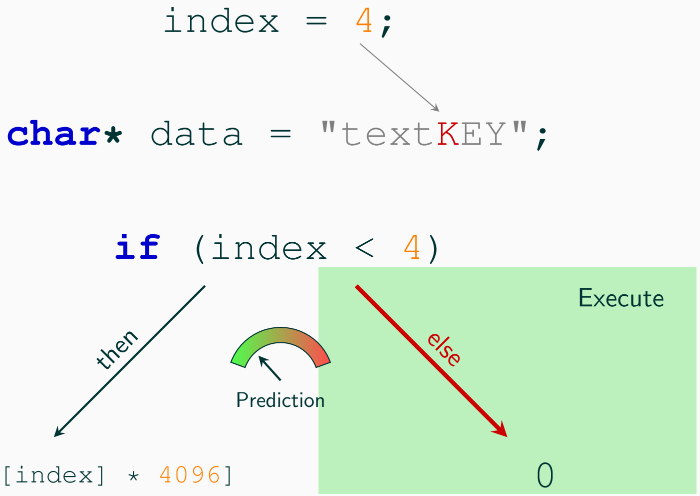


Spectre (variant 1)

```
index = 4;

char* data = "textKEY";

if (index < 4)
```

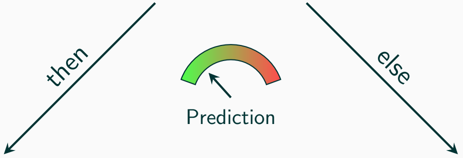


Spectre (variant 1)

```
index = 5;

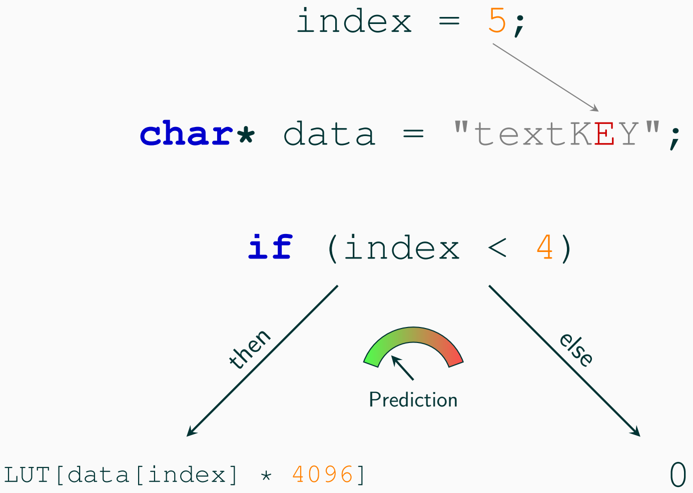
char* data = "textKEY";

if (index < 4)
```

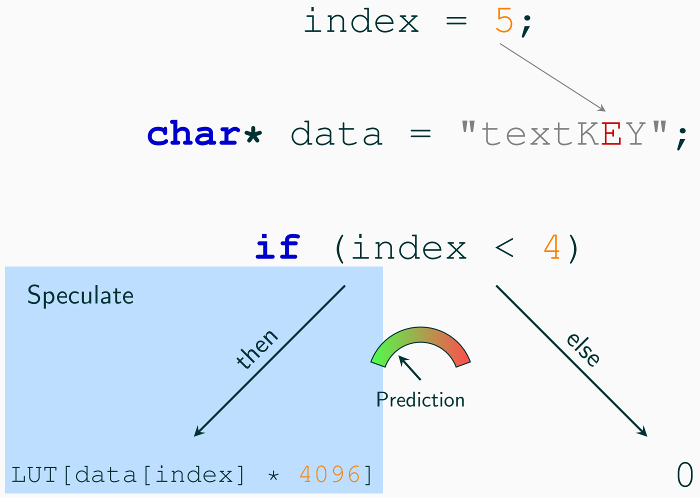


```
LUT[data[index] * 4096]                0
```

Spectre (variant 1)



Spectre (variant 1)



```
index = 5;

char* data = "textKEY";

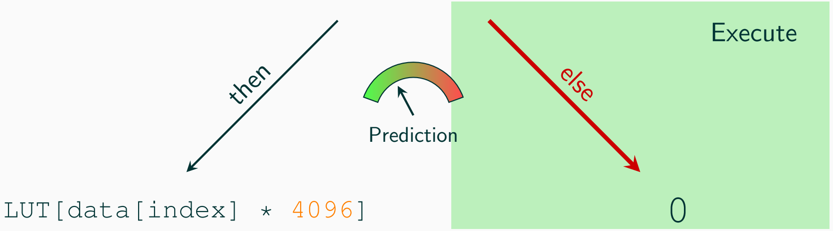
if (index < 4)
```

Spectre (variant 1)

```
index = 5;

char* data = "textKEY";

if (index < 4)
```

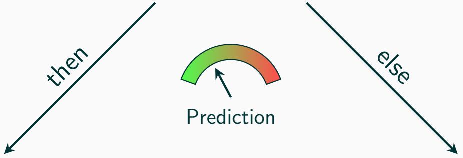


Spectre (variant 1)

```
index = 6;

char* data = "textKEY";

if (index < 4)
```



```
LUT[data[index] * 4096]
```

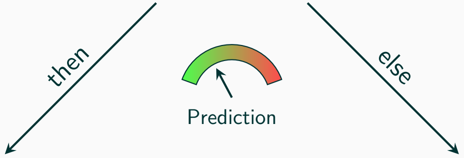
0

Spectre (variant 1)

```
index = 6;

char* data = "textKEY";

if (index < 4)
```



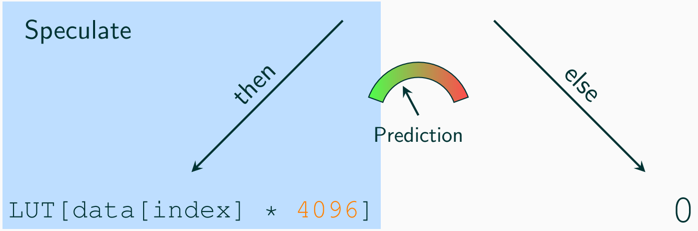
```
LUT[data[index] * 4096]                    0
```

Spectre (variant 1)

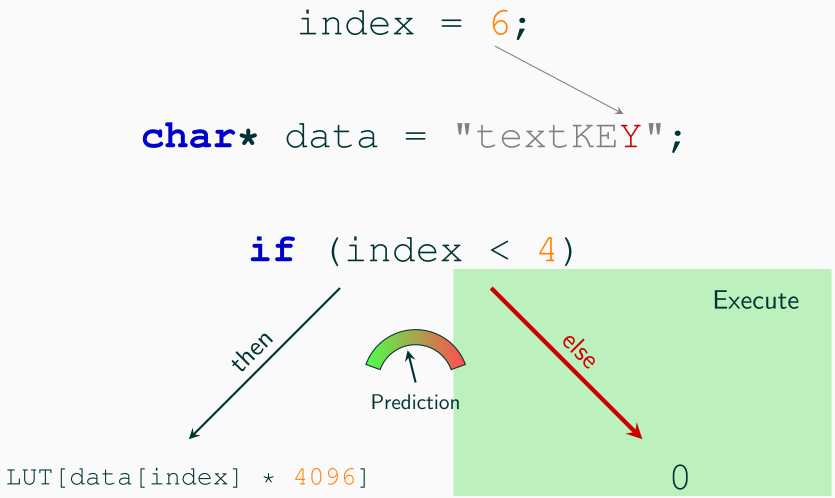
```
index = 6;

char* data = "textKEY";

if (index < 4)
```



Spectre (variant 1)



```
index = 6;

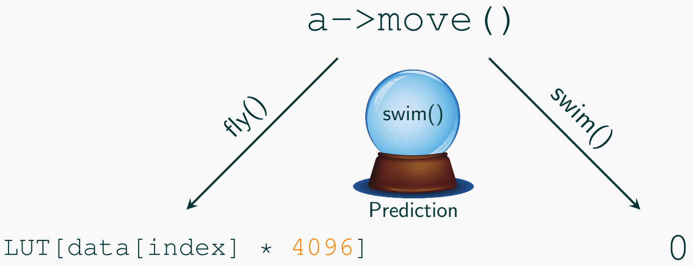
char* data = "textKEY";

if (index < 4)

LUT[data[index] * 4096]                0
```

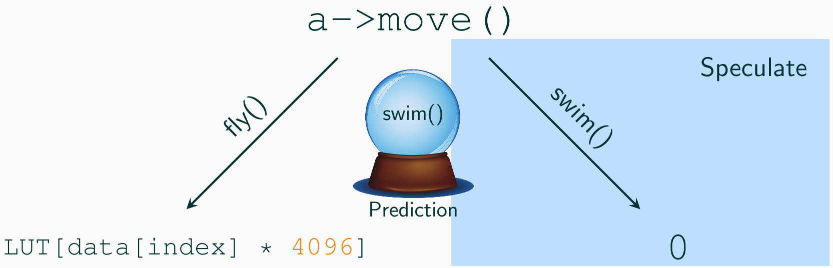
Spectre (variant 2)

```
Animal* a = bird;
```



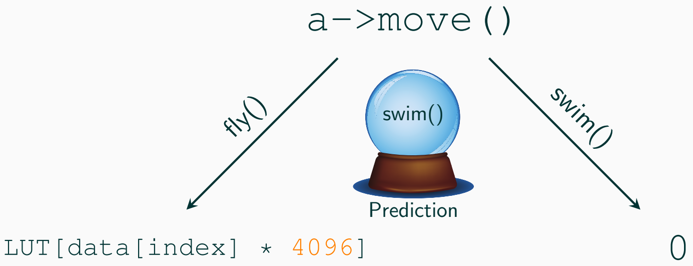
Spectre (variant 2)

```
Animal* a = bird;
```



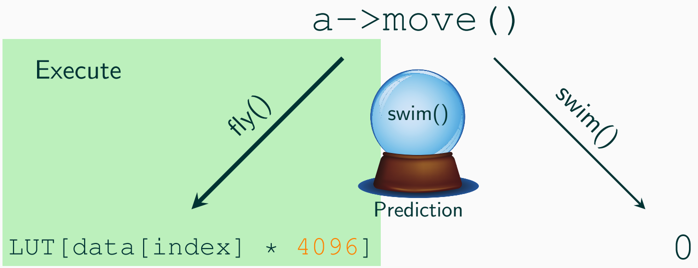
Spectre (variant 2)

```
Animal* a = bird;
```



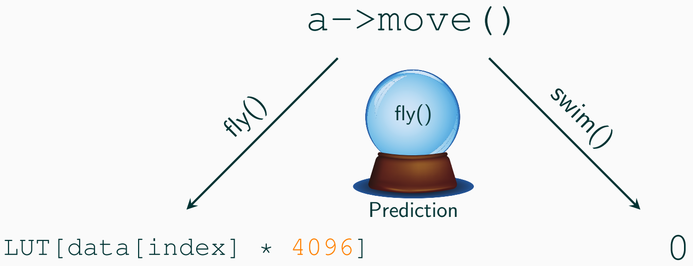
Spectre (variant 2)

```
Animal* a = bird;
```



Spectre (variant 2)

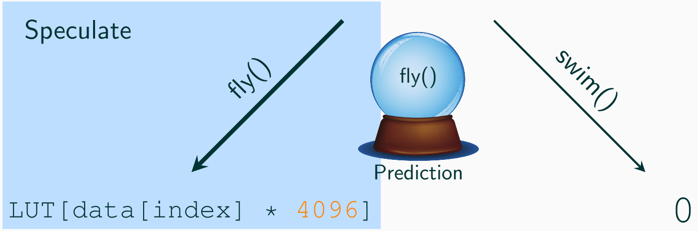
```
Animal* a = bird;
```



Spectre (variant 2)

```
Animal* a = bird;
```

```
a->move()
```

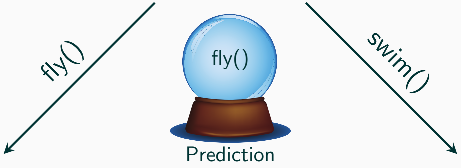


```
LUT[data[index] * 4096]
```

Spectre (variant 2)

```
Animal* a = bird;
```

```
a->move()
```



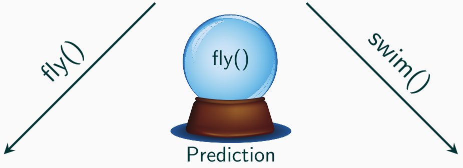
```
LUT[data[index] * 4096]
```

0

Spectre (variant 2)

```
Animal* a = fish;
```

```
a->move()
```

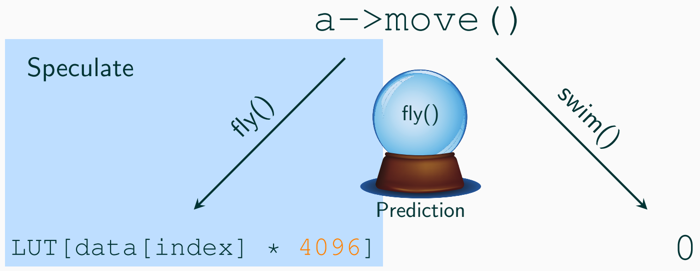


```
LUT[data[index] * 4096]
```

0

Spectre (variant 2)

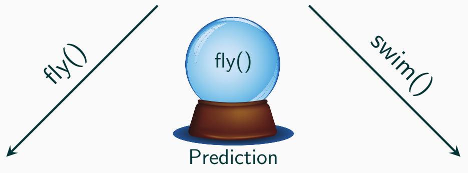
```
Animal* a = fish;
```



Spectre (variant 2)

```
Animal* a = fish;
```

```
a->move()
```



```
LUT[data[index] * 4096]
```

0

Spectre (variant 2)

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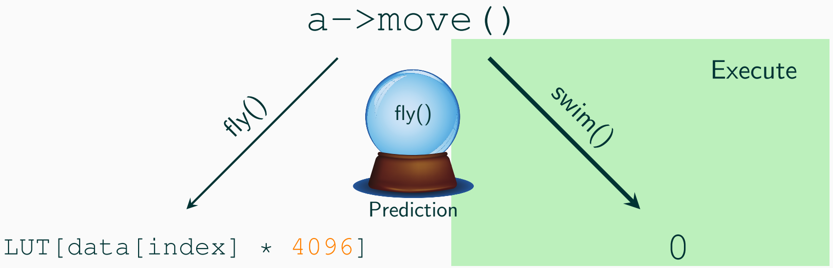

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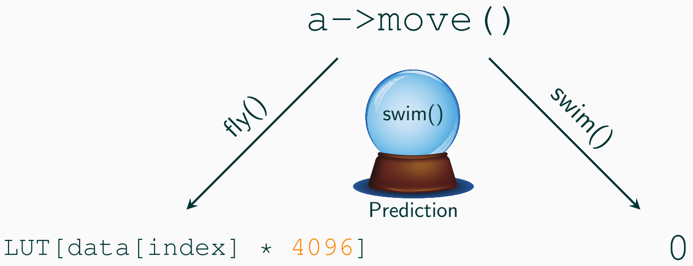

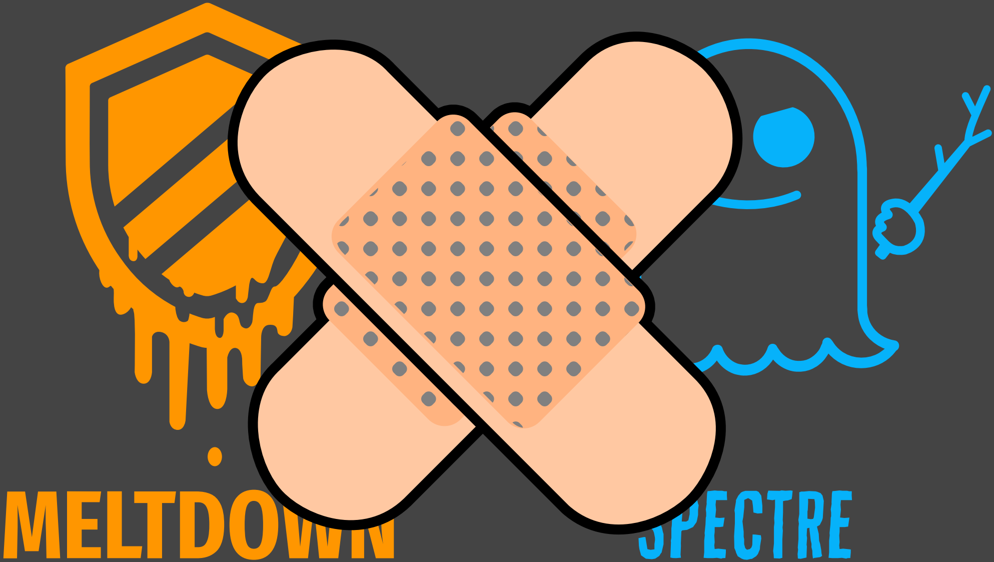
MELTDOWN
SPECTRE

Idea

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- Kernel addresses are then no longer present

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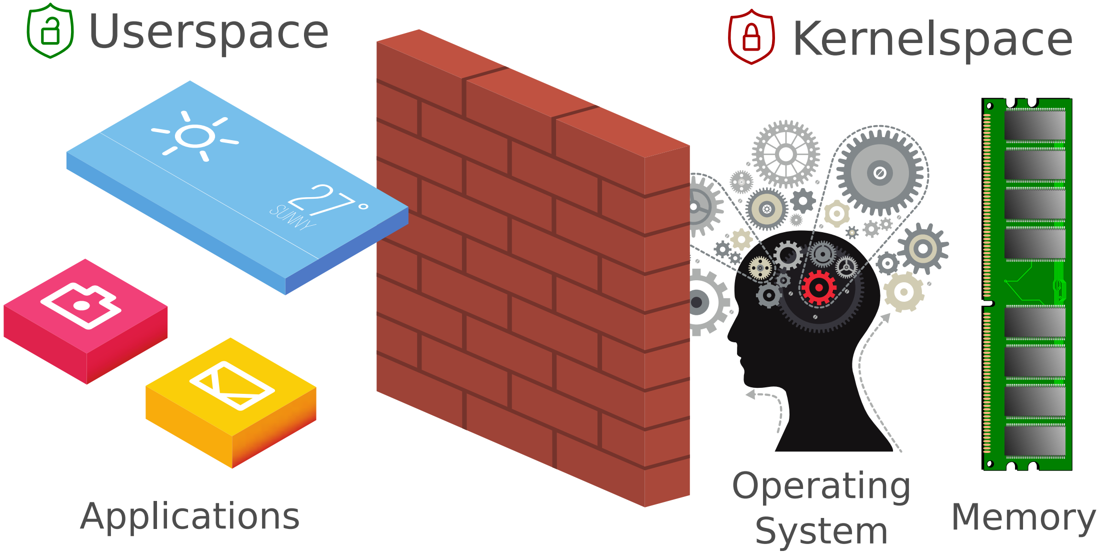
- Kernel addresses are then no longer present
- Memory which is not mapped cannot be accessed at all

Kernel **A**ddress **I**solation to have **S**ide channels **E**fficiently **R**emoved

KAISER /ˈkʌɪzə/

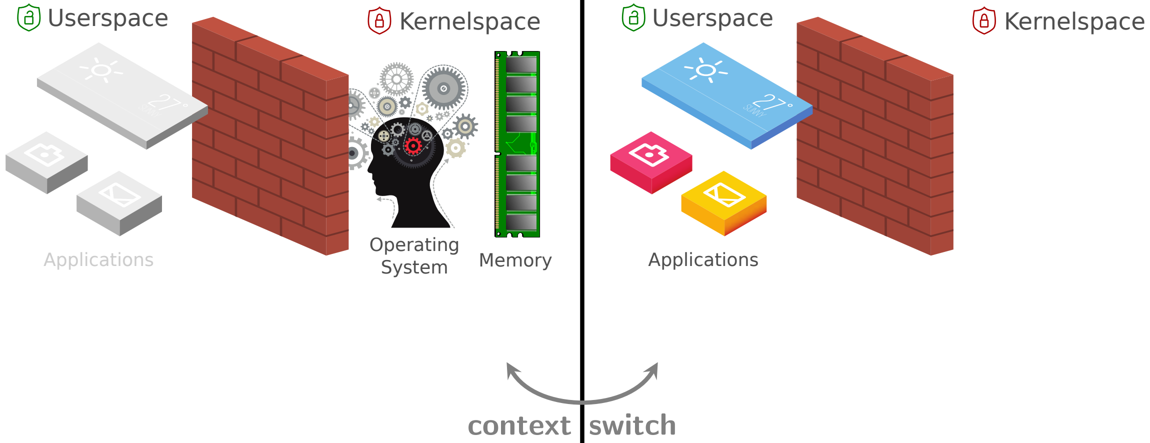
1. [german] Emperor, ruler of an empire
2. largest penguin, emperor penguin

Kernel **A**ddress **I**solation to have **S**ide channels **E**fficiently **R**emoved

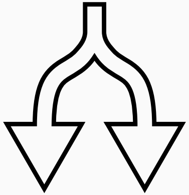

Userspace
Kernelspace
27°
SUNNY
Applications
Operating System
Memory

Kernel View

User View



Kernel Address Space Isolation



- We published KAISER in July 2017

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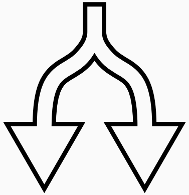

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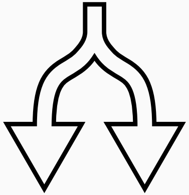

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- Intel and others improved and merged it into Linux as KPTI (Kernel Page Table Isolation)
- Microsoft implemented similar concept in Windows 10
- Apple implemented it in macOS 10.13.2 and called it “Double Map”
- All share the same idea: switching address spaces on context switch

Performance

- Depends on how often you need to switch between kernel and user space

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- ⇒ Performance overhead on average below 2%

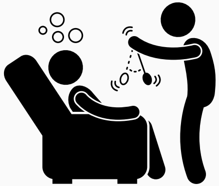
Meltdown and Spectre

MELTDOWN

SPECTRE

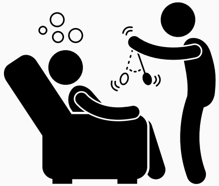
~~Meltdown and~~ Spectre

Spectre



- Does not directly access kernel

Spectre



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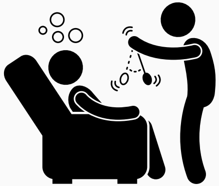

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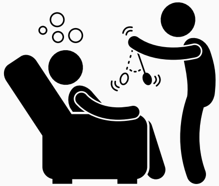

- Does not directly access kernel
- "Convinces" other programs to reveal their secrets
- Much harder to fix, KAISER does not help
- Ongoing effort to patch via microcode update and compiler extensions

Spectre

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- Problem: massive performance hit!
- Also: How to disable it?
- Speculative execution is deeply integrated into CPU

Spectre Variant 1 Mitigations

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Spectre Variant 1 Mitigations

- Workaround: insert instructions stopping speculation

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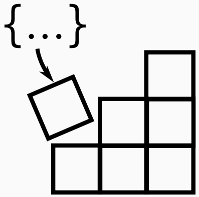
- x86: `LFENCE`, ARM: `CSDB`
- Available on all Intel CPUs, retrofitted to existing ARMv7 and ARMv8

Spectre Variant 1 Mitigations



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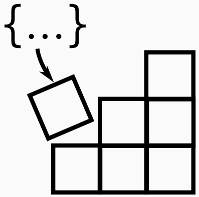

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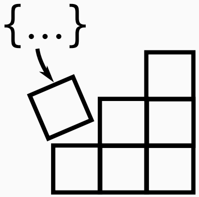

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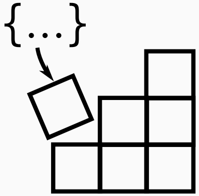

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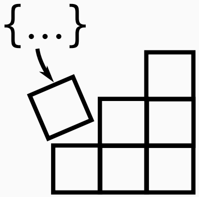

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- Explicit use by programmer: `__builtin_load_no_speculate`

Spectre Variant 1 Mitigations

```
// Unprotected

int array[N];

int get_value(unsigned int n) {
  int tmp;

  if (n < N) {
    tmp = array[n]
  } else {
    tmp = FAIL;
  }

  return tmp;
}
```

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int array[N];

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}
```

```
// Protected

int array[N];

int get_value(unsigned int n) {

  int *lower = array;
  int *ptr = array + n;
  int *upper = array + N;

  return
    __builtin_load_no_speculate
    (ptr, lower, upper, FAIL);

}
```

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Spectre Variant 2 Mitigations (Microcode/MSRs)

Intel released microcode updates

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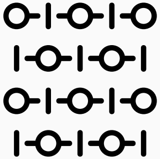

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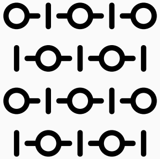

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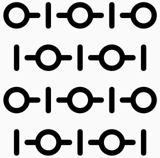

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- Indirect Branch Predictor Barrier (IBPB):
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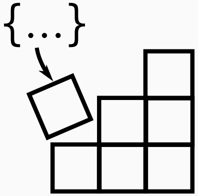
- Single Thread Indirect Branch Predictors (STIBP):
    - Isolates branch prediction state between two hyperthreads

Spectre Variant 2 Mitigations (Software)

Retpoline (compiler extension)



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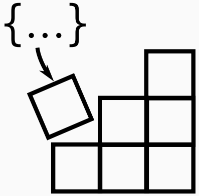

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  push <call_target>
  call 1f
2:                     ; speculation will continue here
  lfence               ; speculation barrier
  jmp 2b               ; endless loop
1:
  lea 8(%rsp), %rsp    ; restore stack pointer
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→ always predict to enter an endless loop

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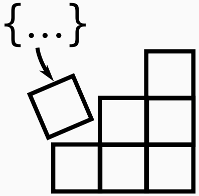

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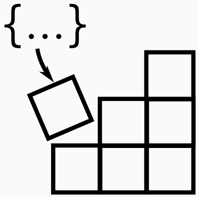

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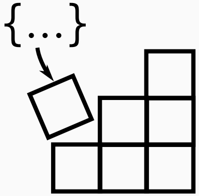

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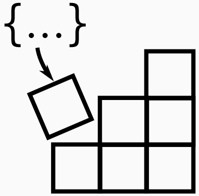

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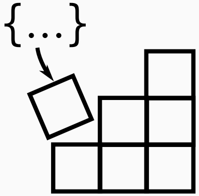

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  → microcode patches to prevent that

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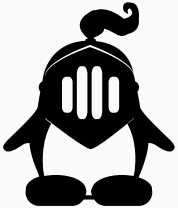

- ARM provides hardened Linux kernel

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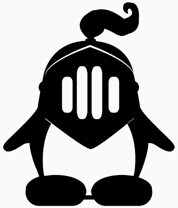

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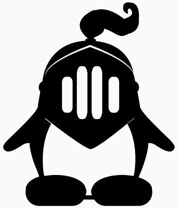

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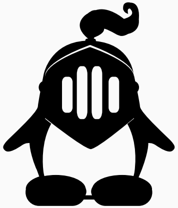

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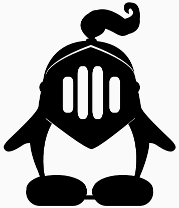

- ARM provides hardened Linux kernel
- Clears branch-predictor state on context switch
- Either via instruction (`BPIALL`)...
- ...or workaround (disable/enable MMU)
- Non-negligible performance overhead ($\approx$ 200-300 ns)

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- Just move secrets into secure world

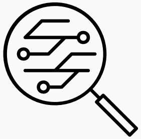
→ Spectre works on secure enclaves

What to do now?

Don’t panic

- Is the used hardware even affected?

Don’t panic



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Don’t panic

- Is the used hardware even affected?
- Can untrusted users run code on affected hardware?
- Is a software attack even in the threat model?
- Is confidentiality required on the hardware?

Learn from it

We have ignored software side-channels for many many years:

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- attacks on ASLR $\rightarrow$ “ASLR is broken anyway”
- attacks on SGX and TrustZone $\rightarrow$ “not part of the threat model”

Learn from it

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- attacks on crypto → "software should be fixed"
- attacks on ASLR → "ASLR is broken anyway"
- attacks on SGX and TrustZone → "not part of the threat model"

→ for years we solely optimized for performance

When you read the manuals...

After learning about a side channel you realize:

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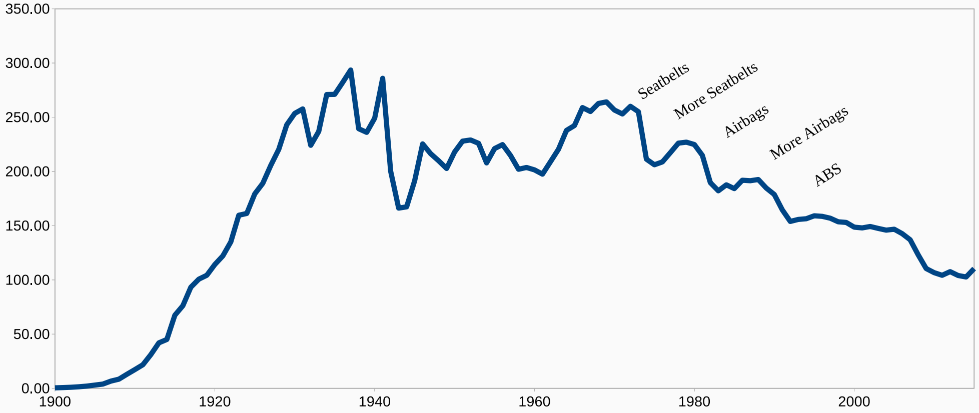
- the side channels were documented in the Intel manual

When you read the manuals...

After learning about a side channel you realize:

- the side channels were documented in the Intel manual
- only now we understand the implications

What do we learn from it?



Motor Vehicle Deaths in U.S. by Year

A unique chance

A unique chance to

- rethink processor design
- grow up, like other fields (car industry, construction industry)
- find good trade-offs between security and performance

Conclusion

- Underestimated microarchitectural attacks for a long time
  - Basic techniques were there for years
- Industry and customers must embrace security mechanisms
  - Run through the same development (for security) as the automobile industry (for safety)
  - It should not be “performance first”, but “security first”

Any Questions?

Spectre and Meltdown on x86 and ARM

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