Malware Guard Extension: Using SGX to Conceal Cache Attacks

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Graz University of Technology

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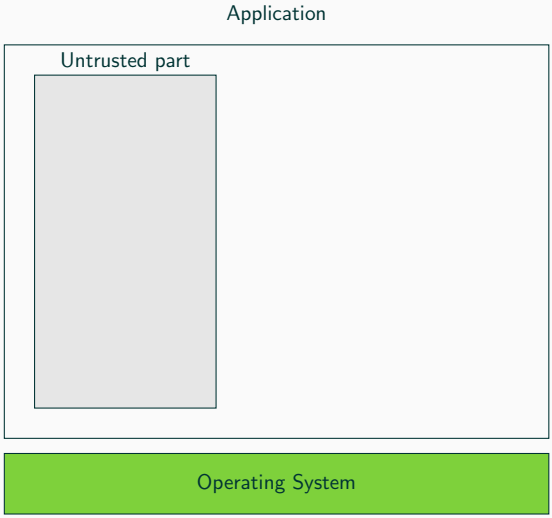
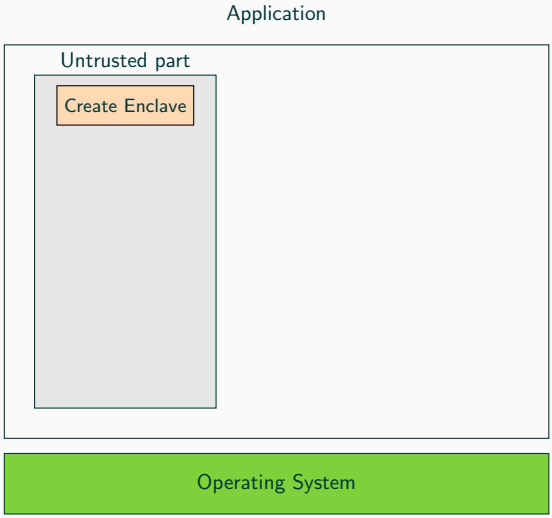
- We discuss countermeasures to prevent such attacks

Background


Application
Untrusted part
Operating System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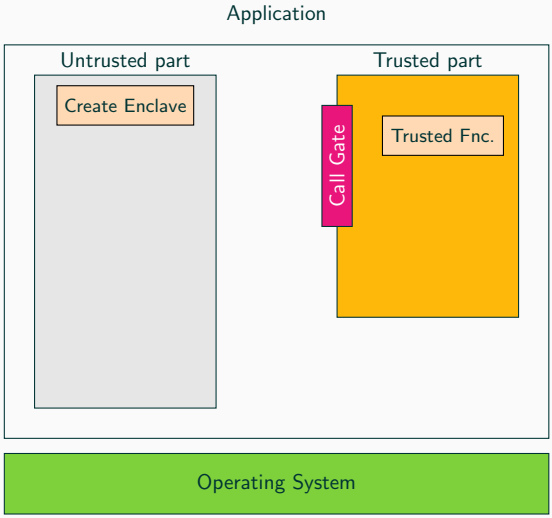
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Trusted Fnc.
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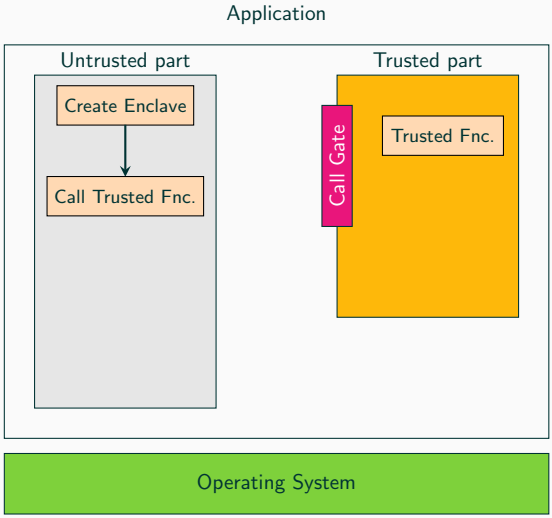
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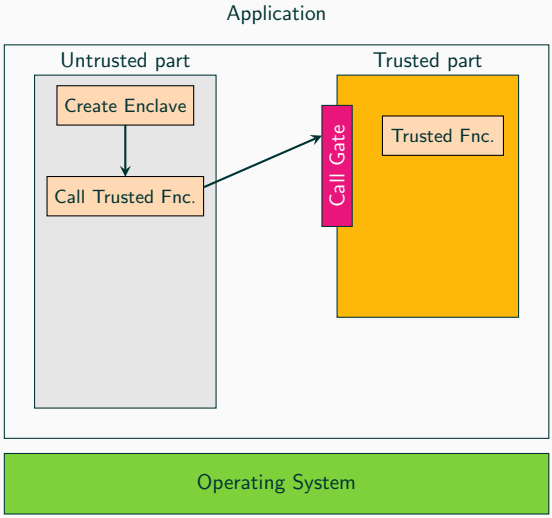
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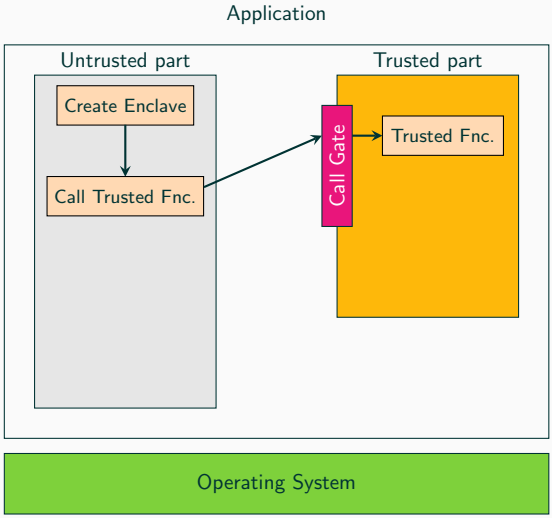
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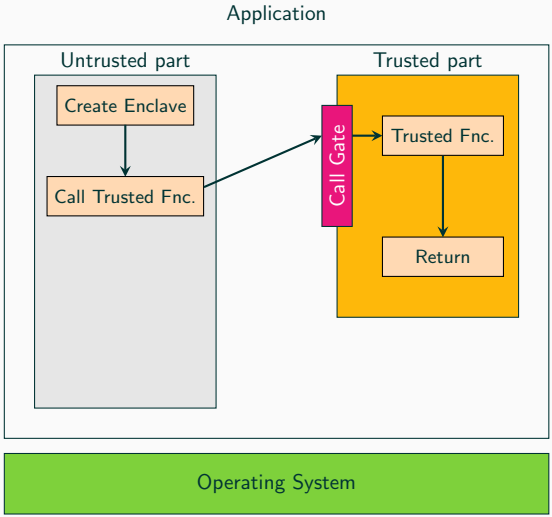
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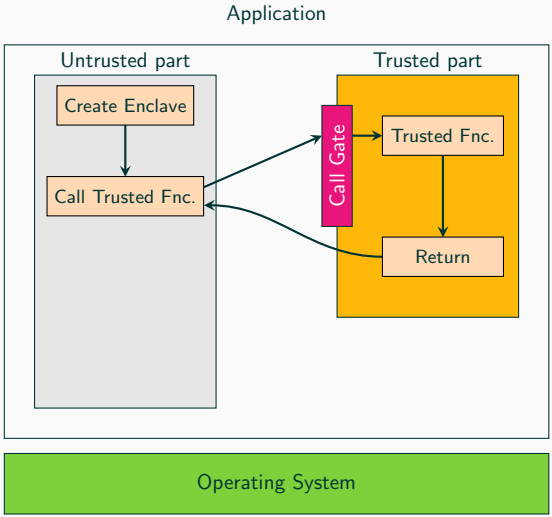
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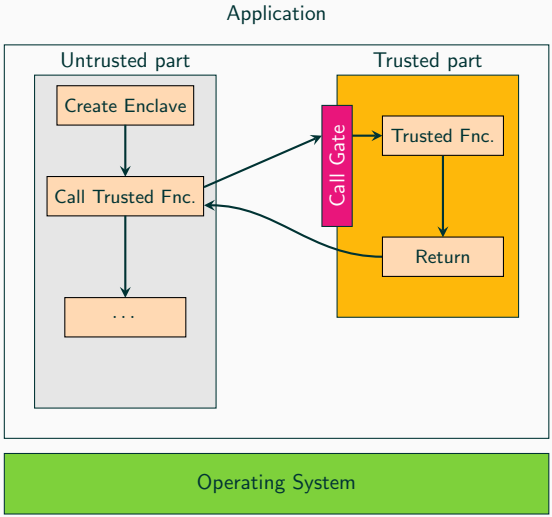
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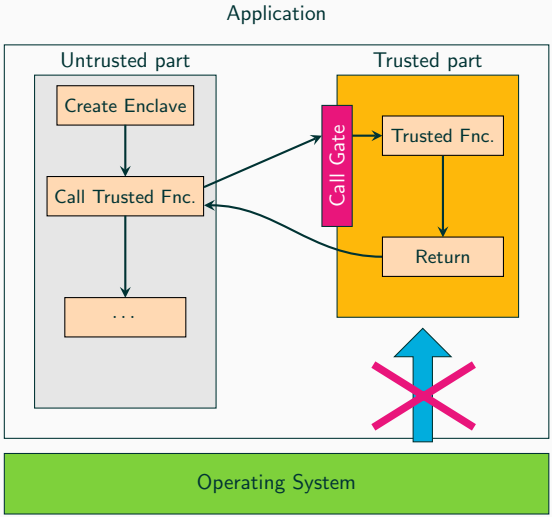
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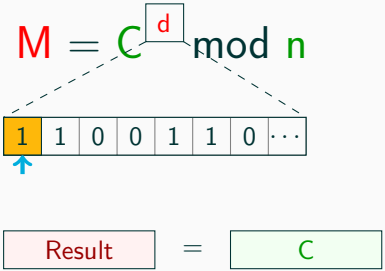
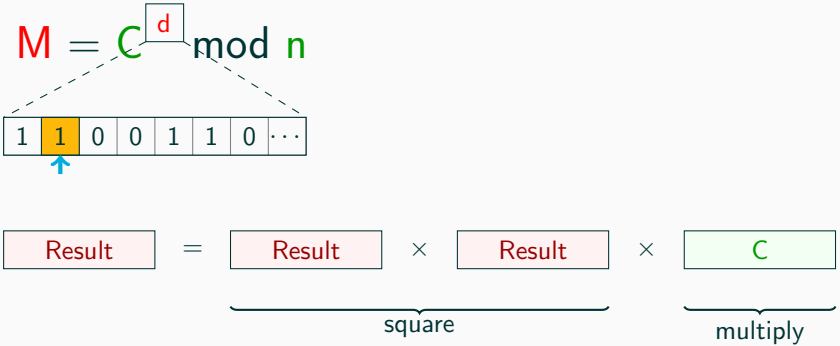

M = C^d mod n
1 1 0 0 1 1 0 ···
Result = C


M = C^d mod n
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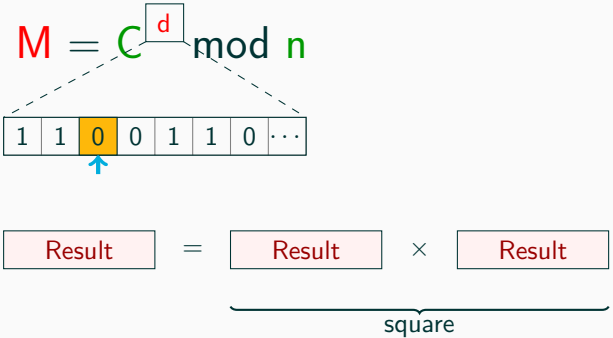
Result = Result × Result × C
square
multiply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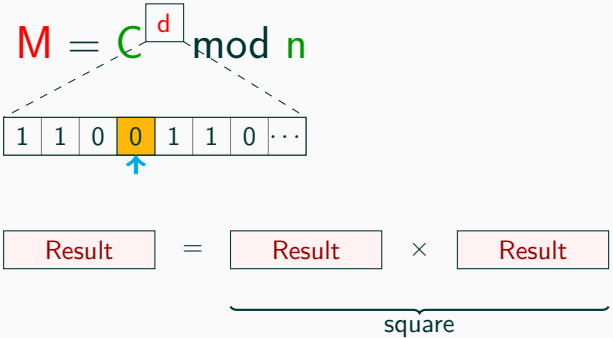
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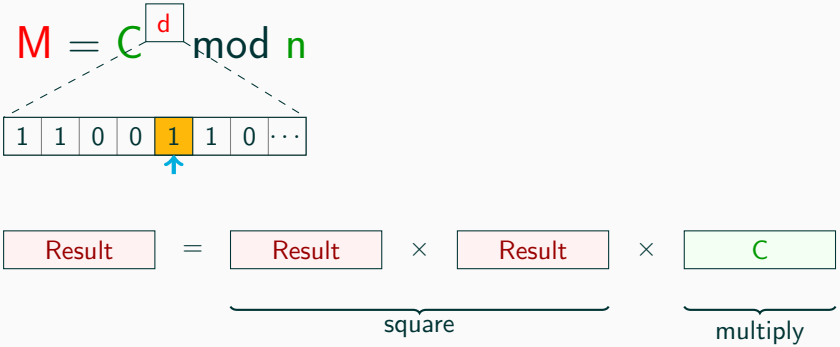
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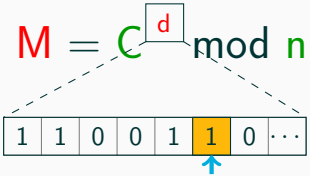
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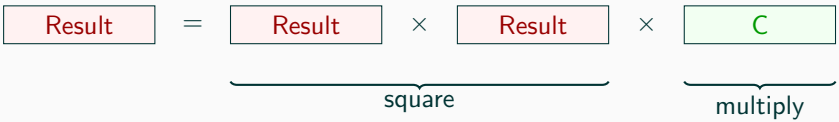
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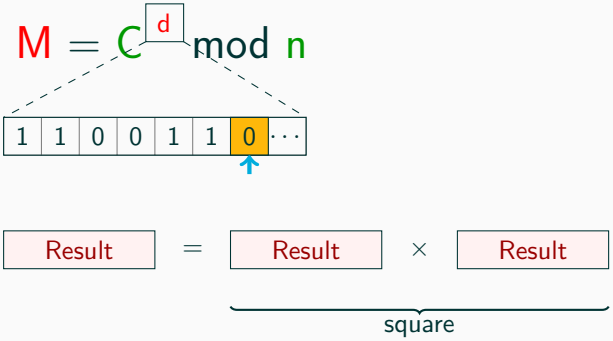
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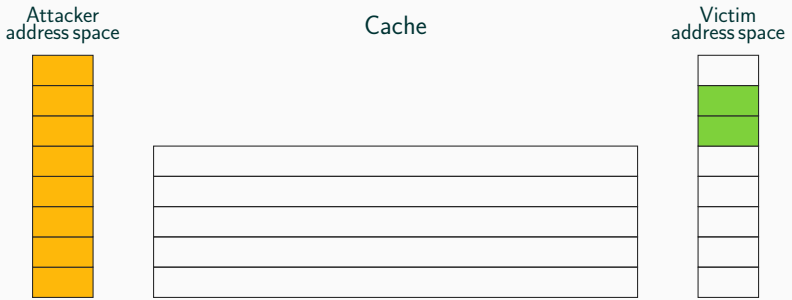
- works across CPU cores as the last-level cache is shared



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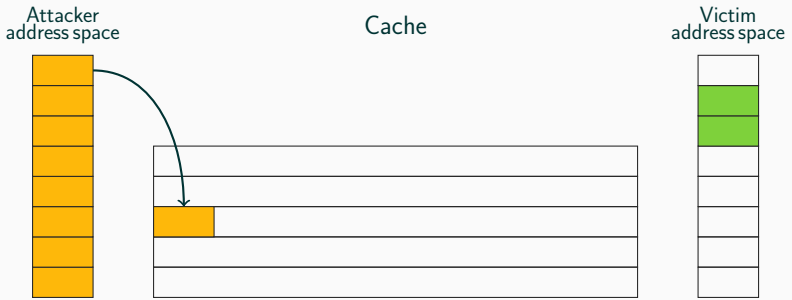

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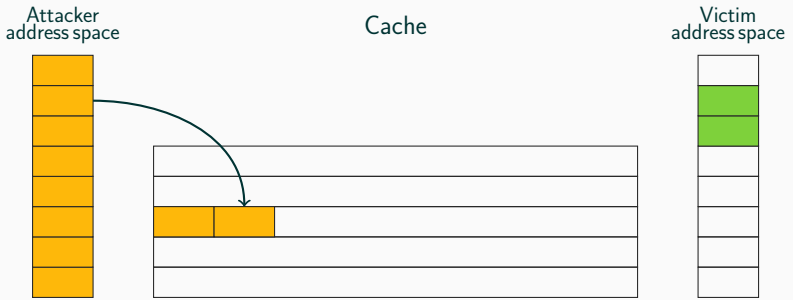

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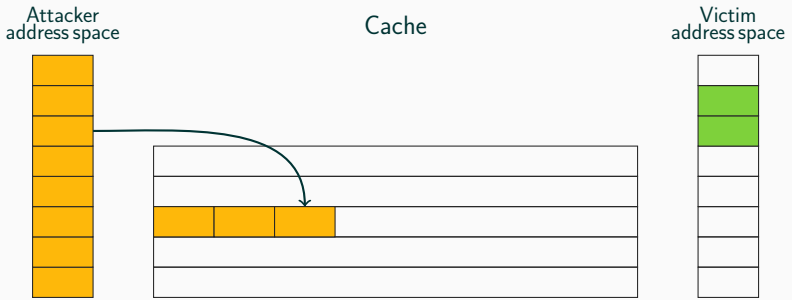

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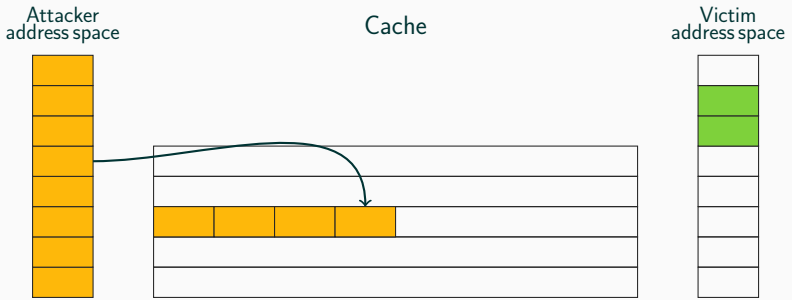

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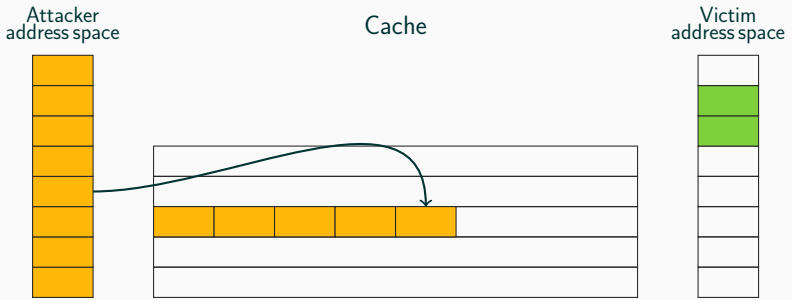

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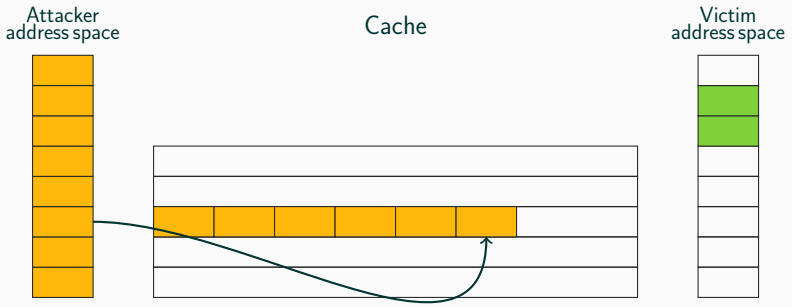

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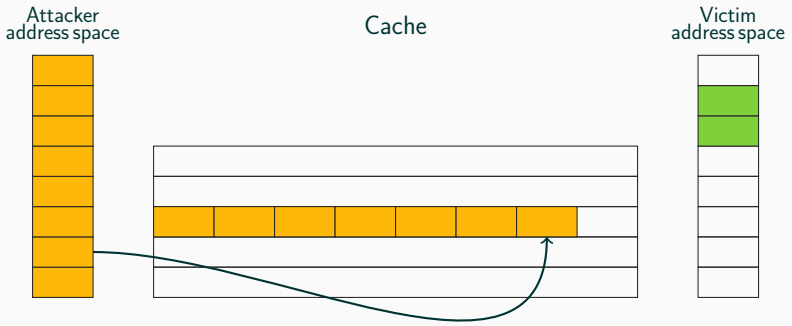

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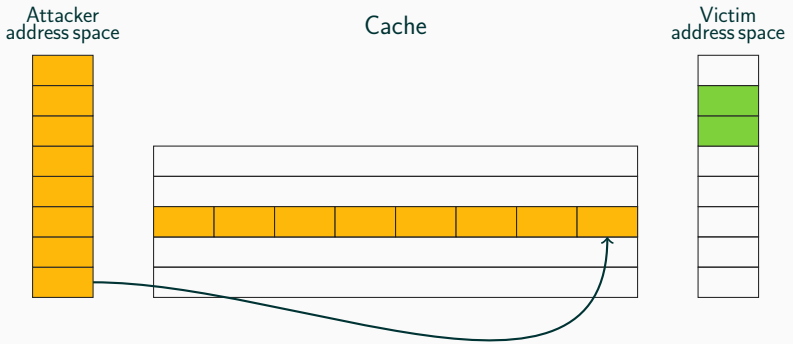

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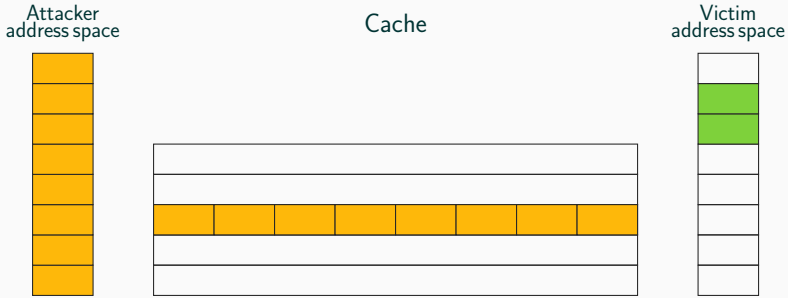

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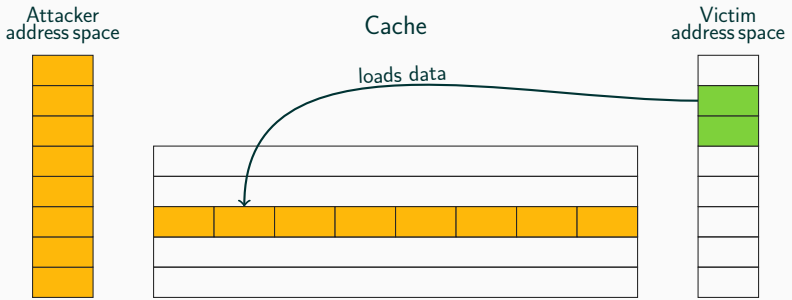

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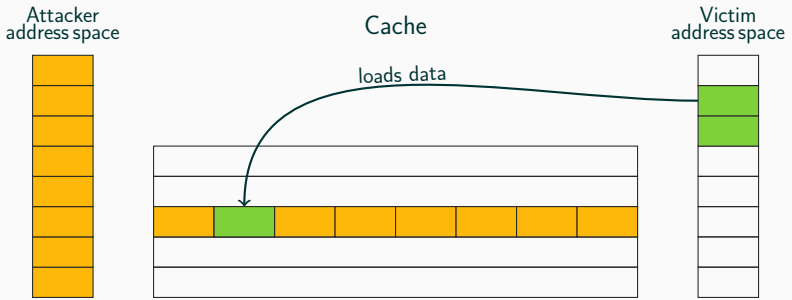

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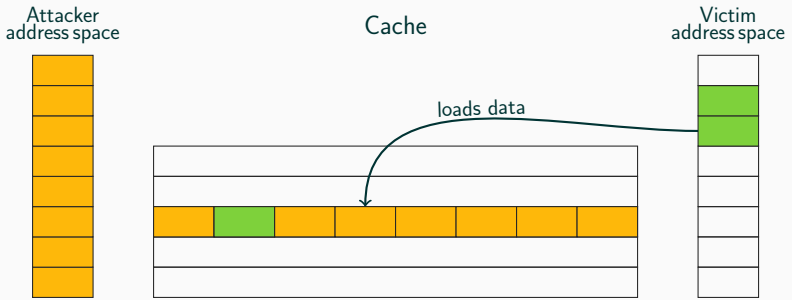

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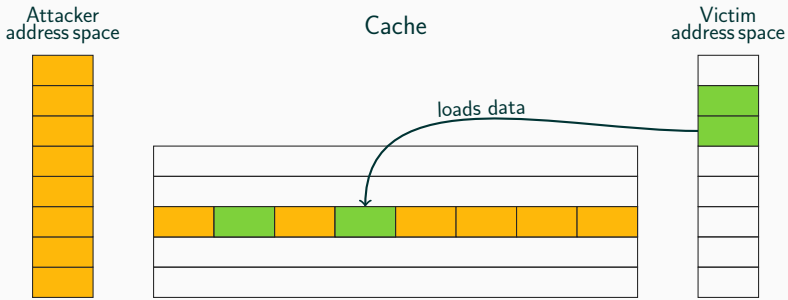

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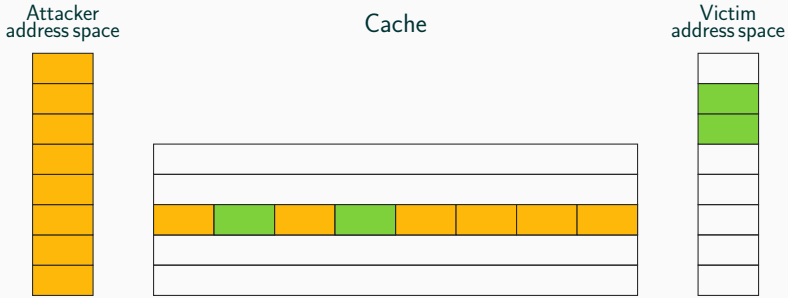

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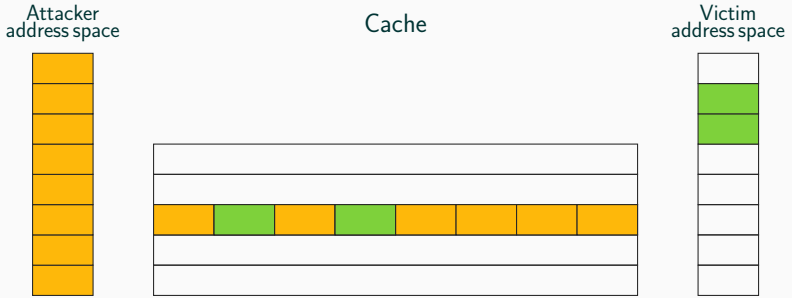

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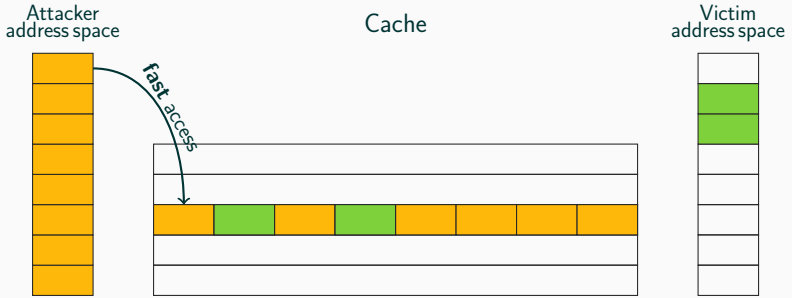

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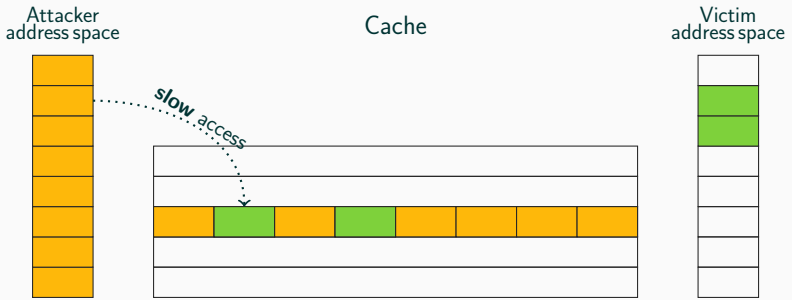

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Attack

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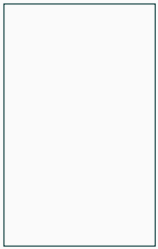
Victim



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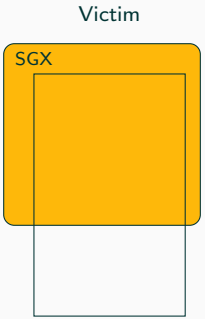

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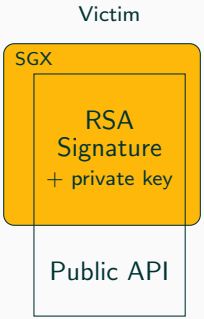

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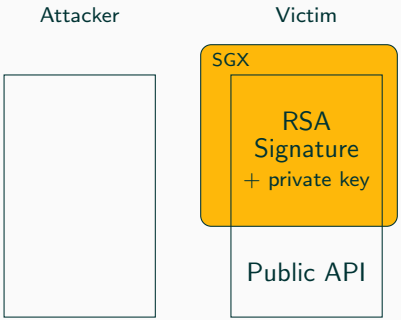

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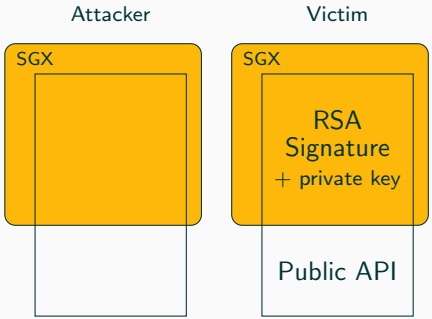

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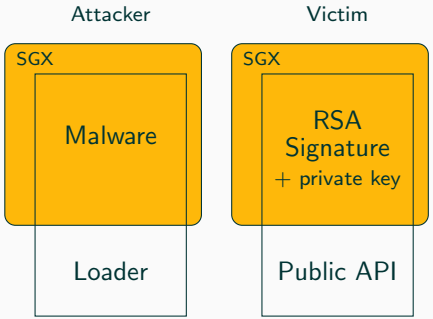

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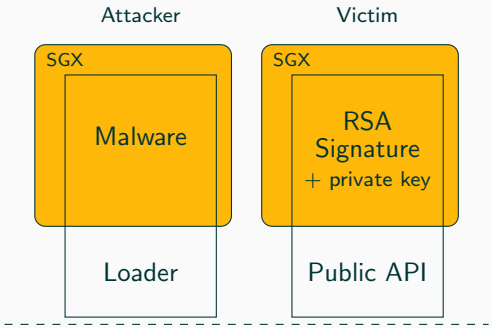

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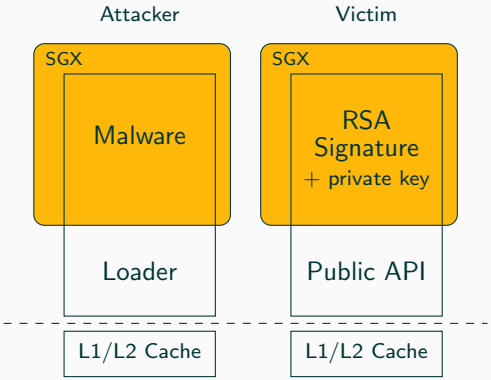

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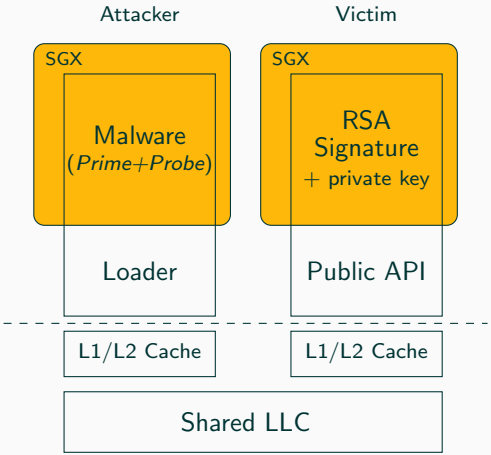

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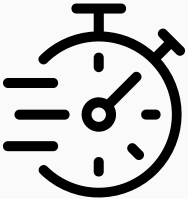

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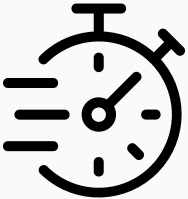

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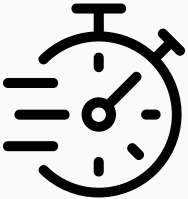

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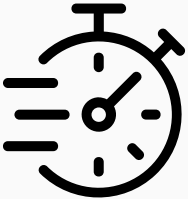
- Start a thread that continuously increments a global variable

Timer



- We have to build our own timer
- Timer resolution must be in the order of cycles
- Start a thread that continuously increments a global variable
- The global variable is our timestamp

Timer

CPU cycles one increment takes

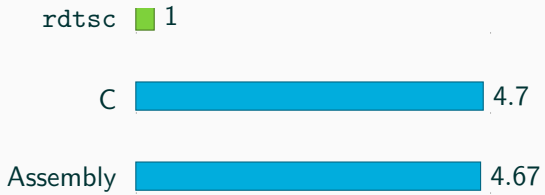
`rdtsc` 1

```
1 timestamp = rdtsc();
```

CPU cycles one increment takes

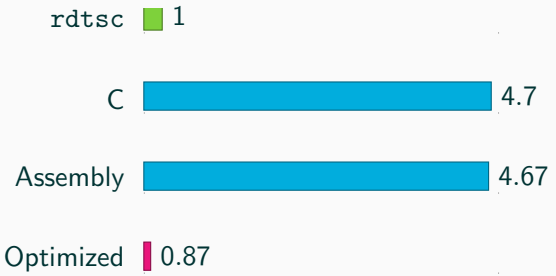

```
1 while(1) {
2   timestamp++;
3 }
```

CPU cycles one increment takes

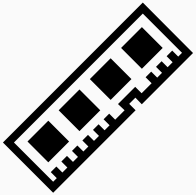



```
1 mov &timestamp, %rcx
2 1: incl (%rcx)
3 jmp 1b
```

CPU cycles one increment takes

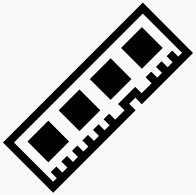



```
1 mov &timestamp, %rcx
2 1: inc %rax
3 mov %rax, (%rcx)
4 jmp 1b
```



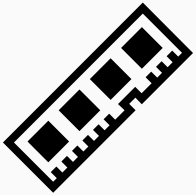
- Cache set is determined by part of physical address

Physical Addresses



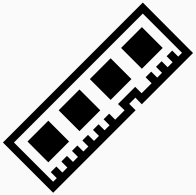
- Cache set is determined by part of physical address
- We have no knowledge of physical addresses

Physical Addresses



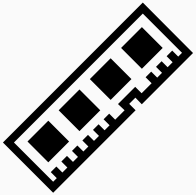
- Cache set is determined by part of physical address
- We have no knowledge of physical addresses
- Use the DRAM mapping reverse engineered by Pessl et al.

Physical Addresses



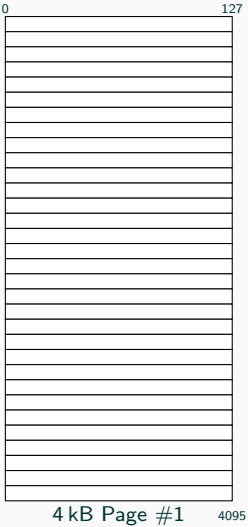
- Cache set is determined by part of physical address
- We have no knowledge of physical addresses
- Use the DRAM mapping reverse engineered by Pessl et al.
- Exploit timing differences to find DRAM row borders

Physical Addresses



- Cache set is determined by part of physical address
- We have no knowledge of physical addresses
- Use the DRAM mapping reverse engineered by Pessl et al.
- Exploit timing differences to find DRAM row borders
- The 18 LSBs are '0' at a row border

Physical Addresses



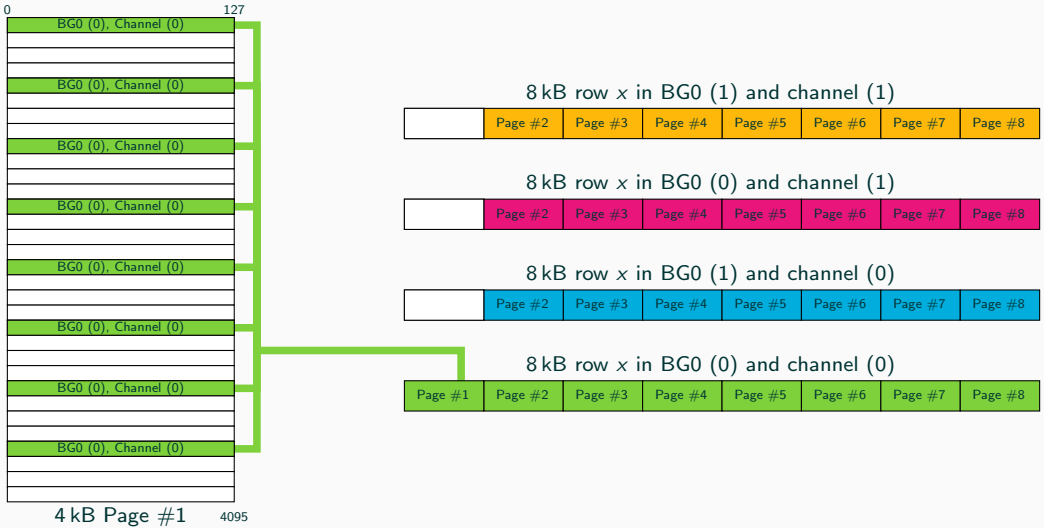
8 kB row x in BG0 (1) and channel (1)

8 kB row x in BG0 (0) and channel (1)

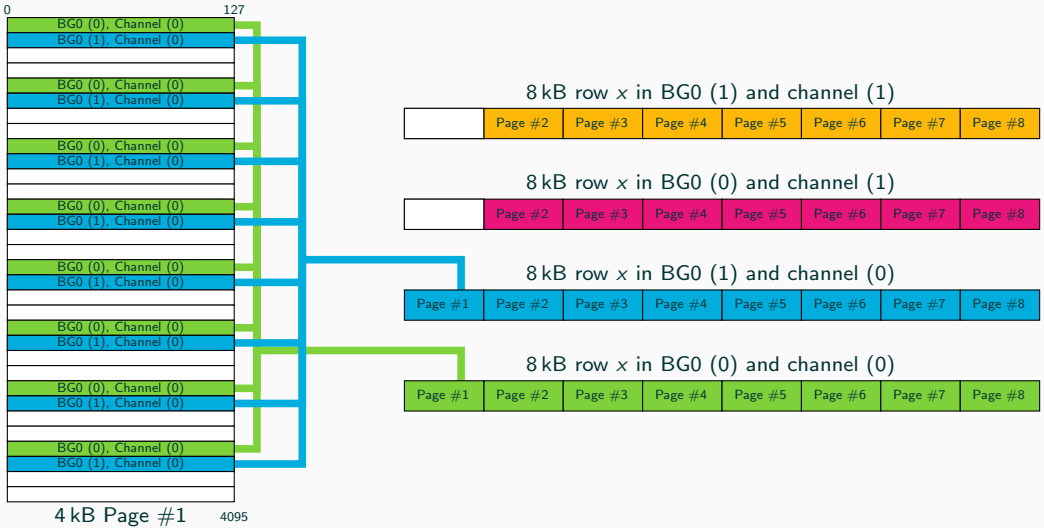
8 kB row x in BG0 (1) and channel (0)

8 kB row x in BG0 (0) and channel (0)

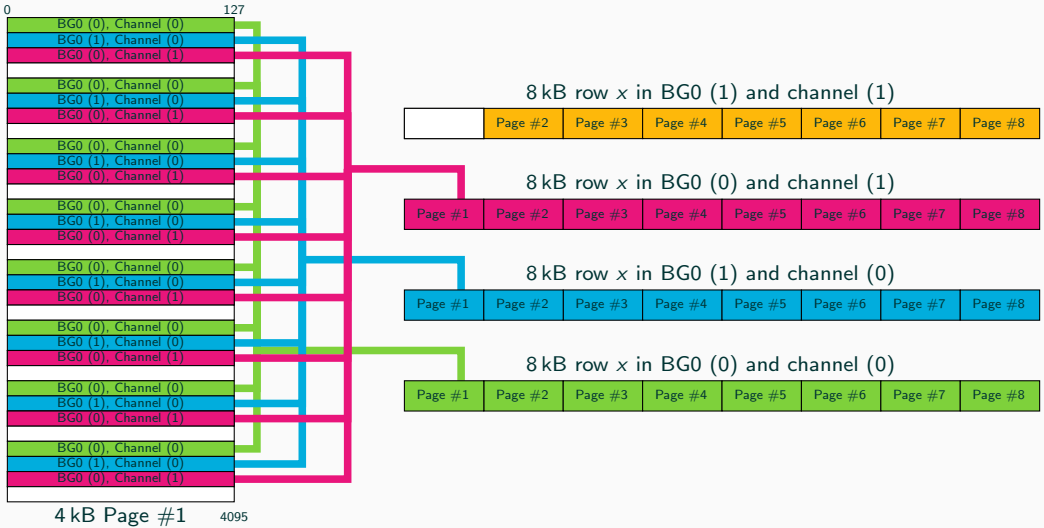
Physical Addresses

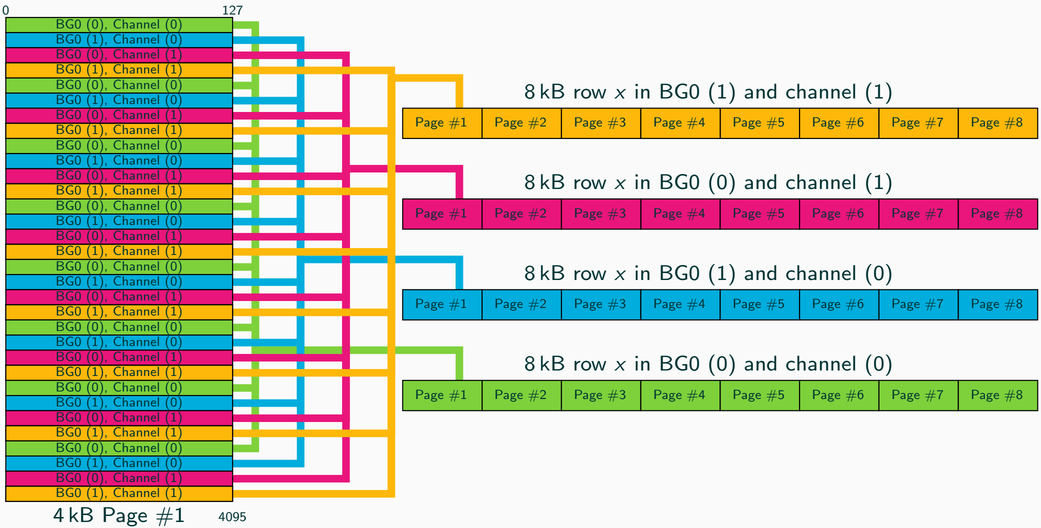


Physical Addresses

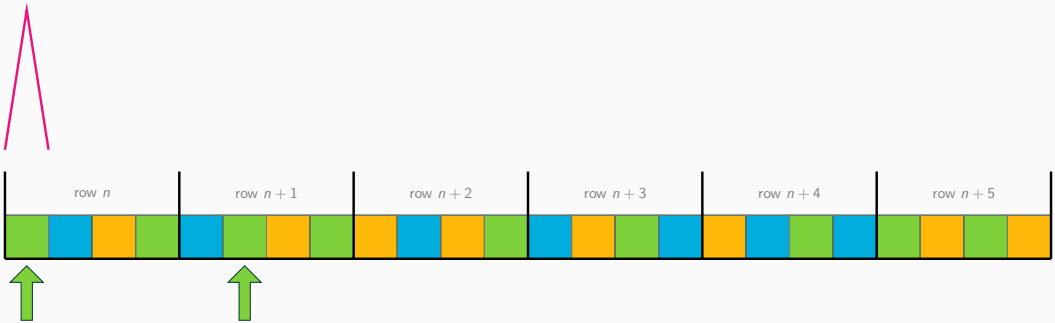


Physical Addresses

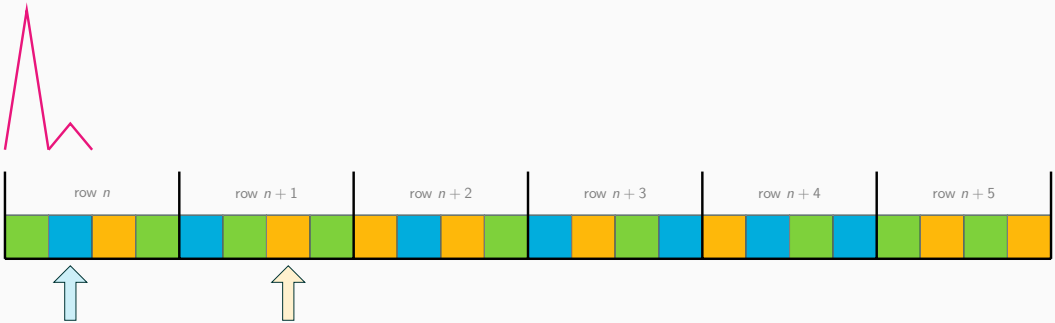


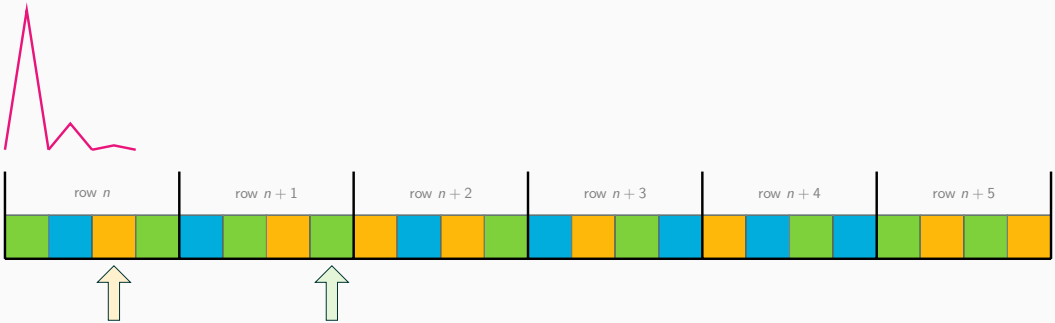

0
127
BG0 (0), Channel (0)
BG0 (1), Channel (0)
BG0 (0), Channel (1)
BG0 (1), Channel (1)
4 kB Page #1
4095
8 kB row x in BG0 (1) and channel (1)
8 kB row x in BG0 (0) and channel (1)
8 kB row x in BG0 (1) and channel (0)
8 kB row x in BG0 (0) and channel (0)
Page #1
Page #2
Page #3
Page #4
Page #5
Page #6
Page #7
Page #8

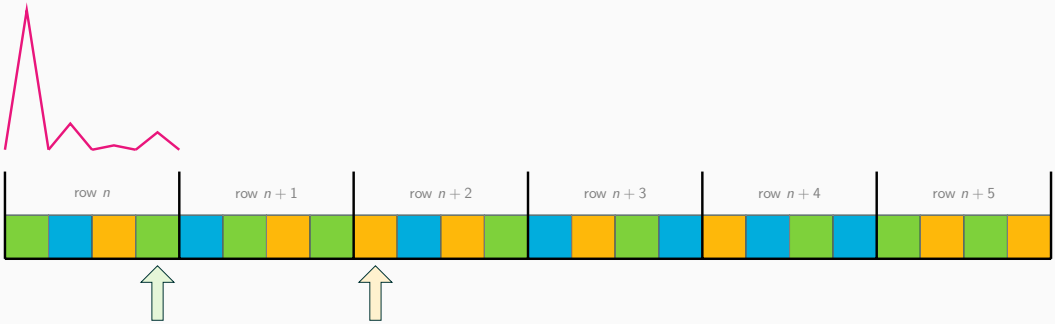
Physical Addresses

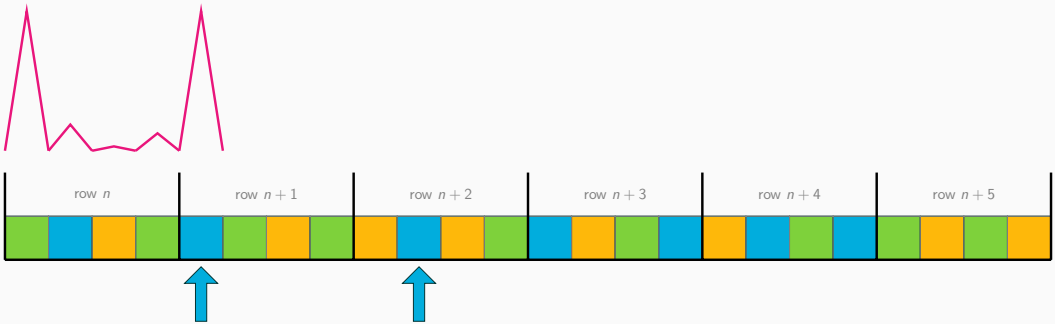


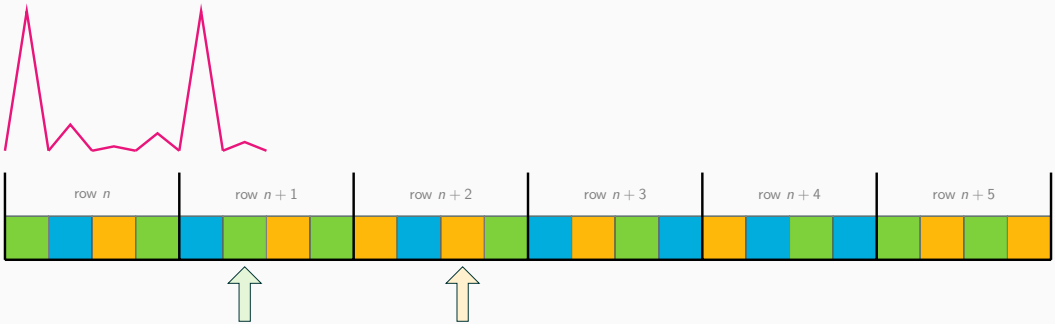
Physical Addresses




row n
row $n+1$
row $n+2$
row $n+3$
row $n+4$
row $n+5$


row n
row $n+1$
row $n+2$
row $n+3$
row $n+4$
row $n+5$


row n
row $n+1$
row $n+2$
row $n+3$
row $n+4$
row $n+5$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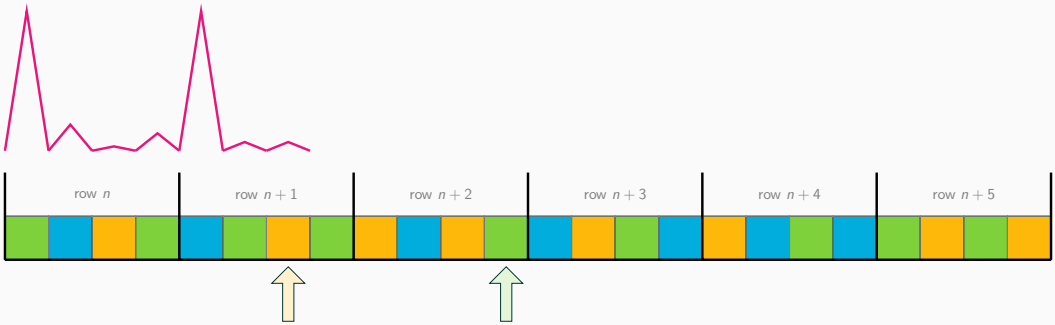
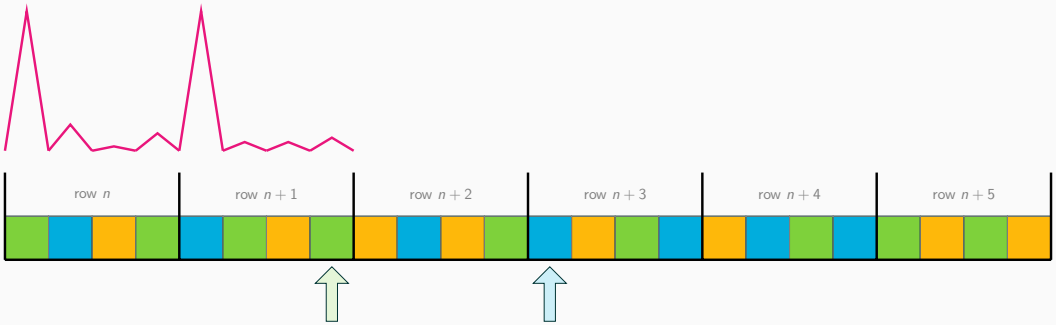
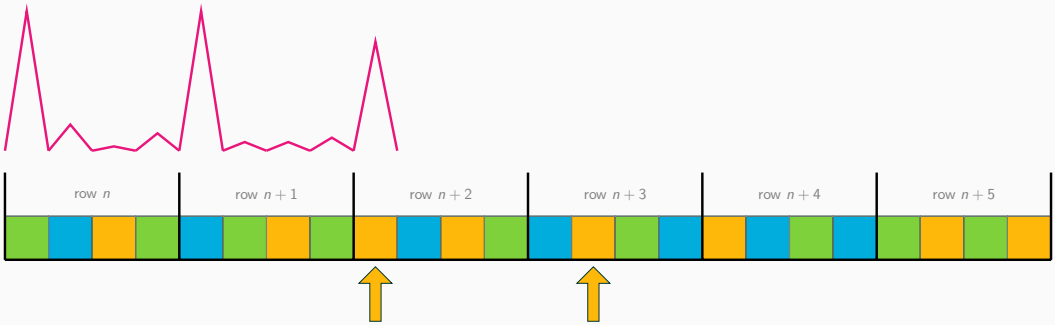
Physical Addresses

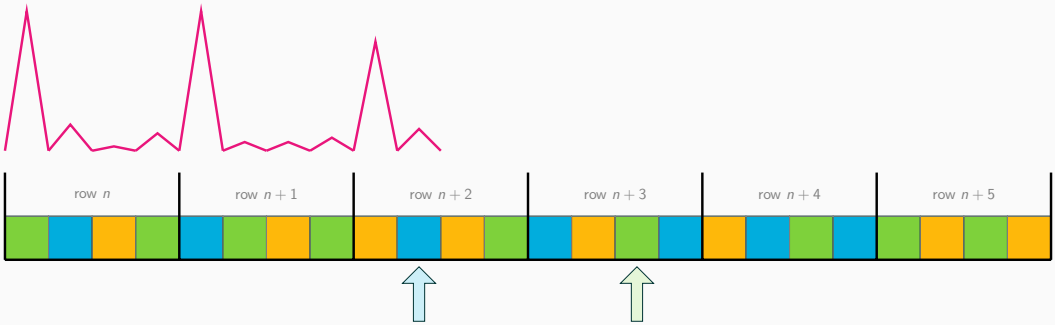



row n
row $n+1$
row $n+2$
row $n+3$
row $n+4$
row $n+5$

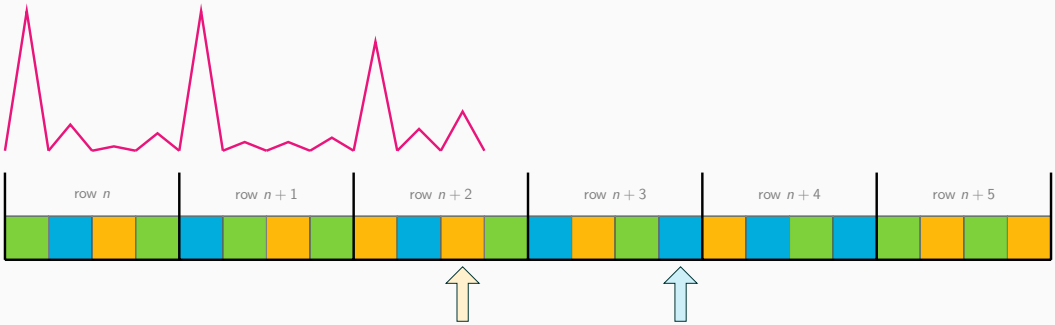
Physical Addresses



Physical Addresses



Physical Addresses



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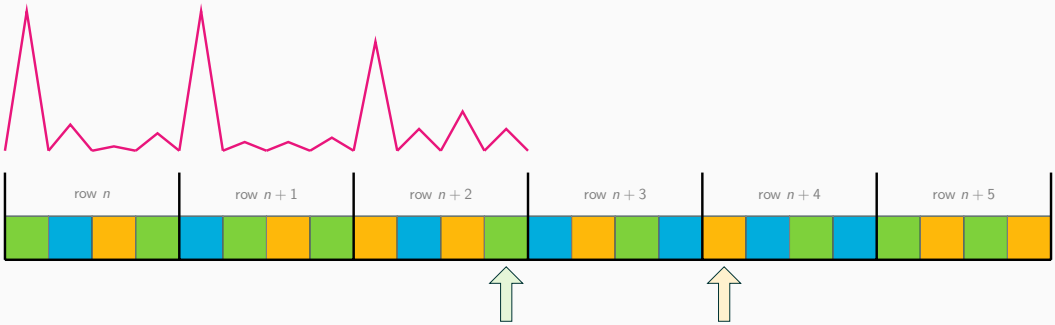
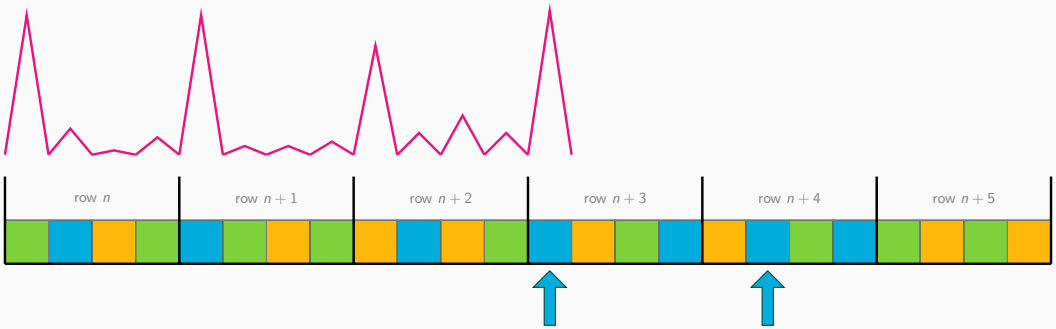
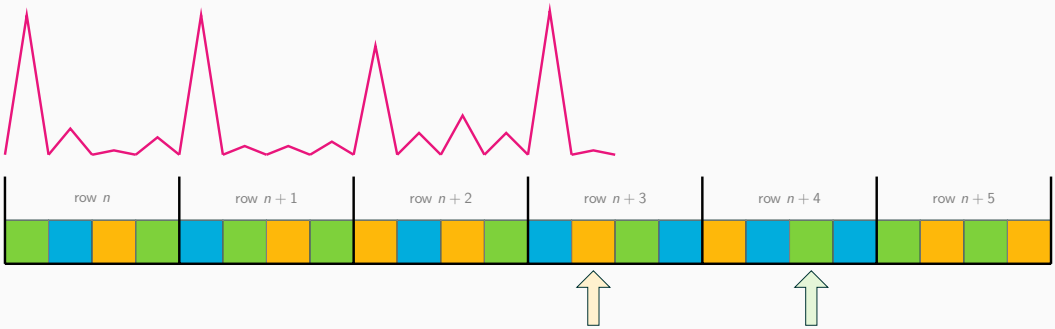


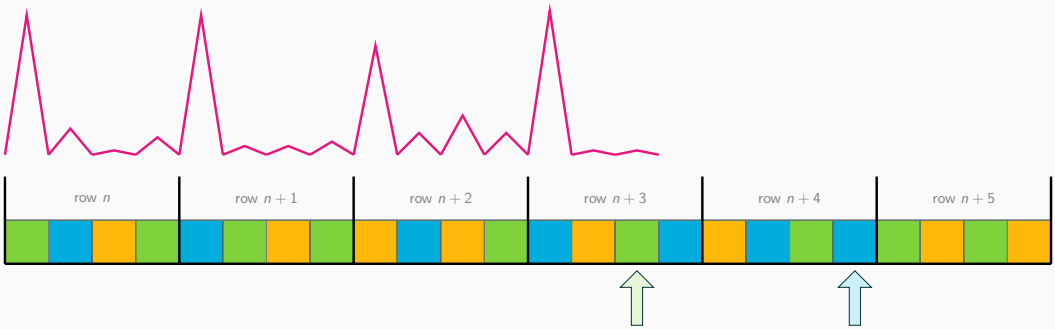
Physical Addresses



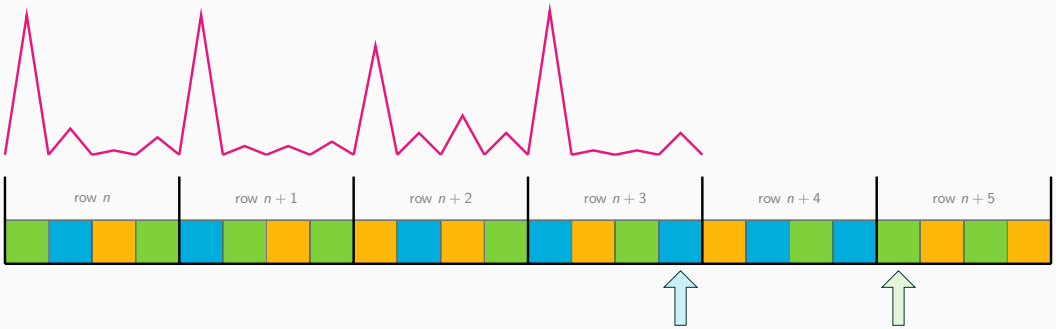
Physical Addresses



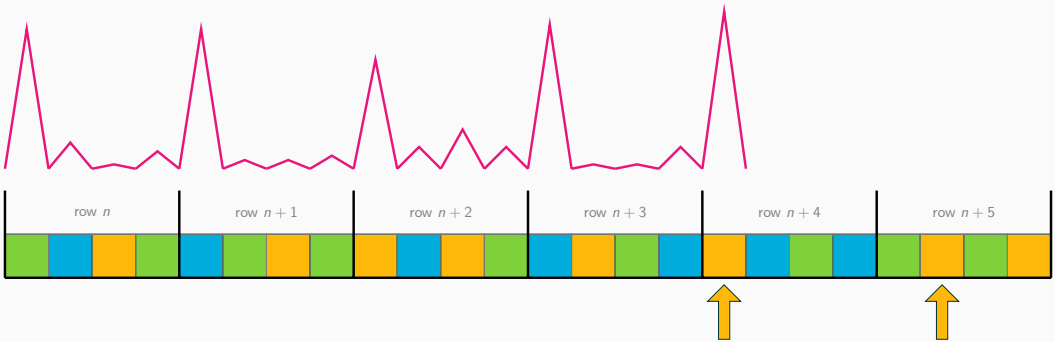
Physical Addresses



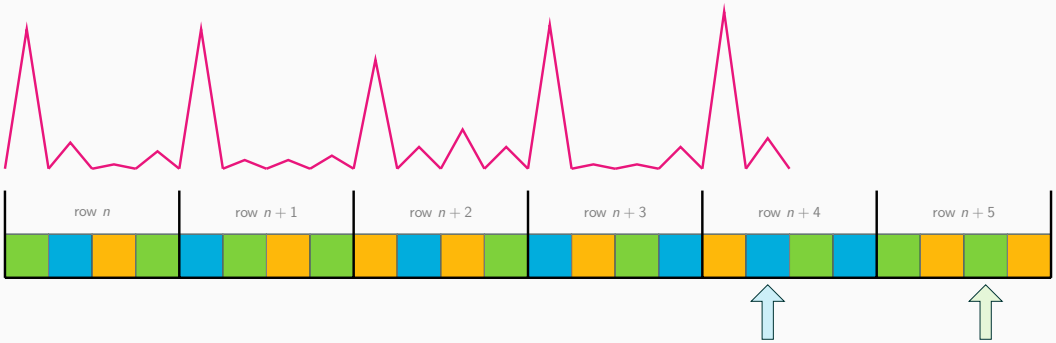
Physical Addresses



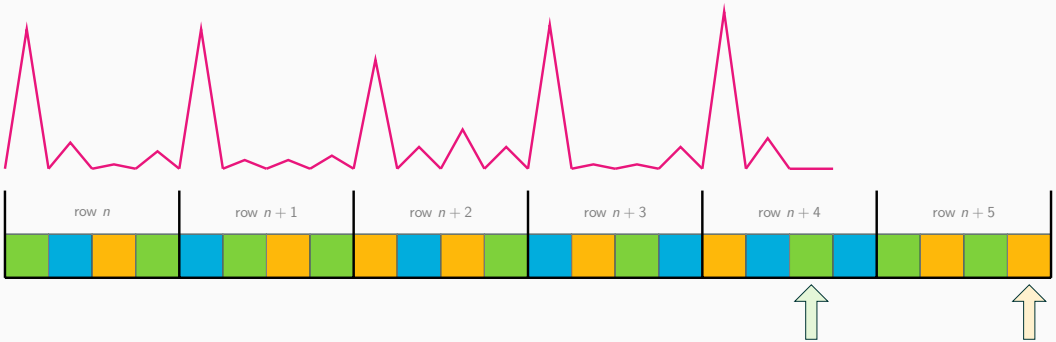
Physical Addresses



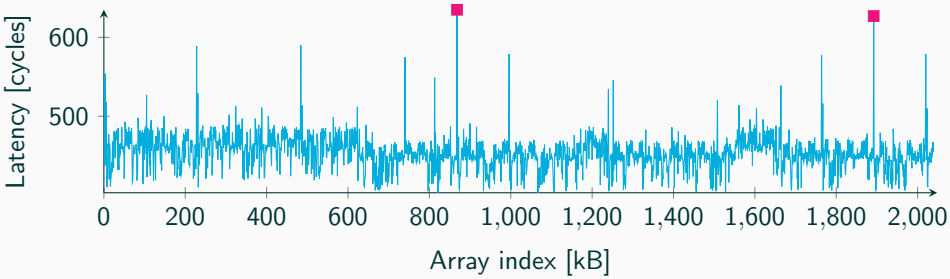
Physical Addresses

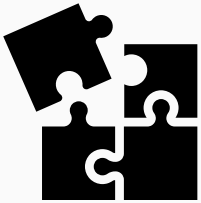


Physical Addresses



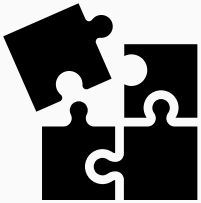
Result on an Intel i5-6200U





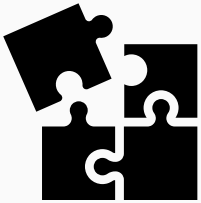
1. Use the counting primitive to measure DRAM accesses

Combining Everything



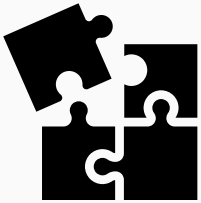
1. Use the counting primitive to measure DRAM accesses
2. Through the DRAM side channel, determine the row borders

Combining Everything



1. Use the counting primitive to measure DRAM accesses
2. Through the DRAM side channel, determine the row borders
3. Row borders have the 18 LSBs set to '0' $\rightarrow$ maps to cache set '0'

Combining Everything



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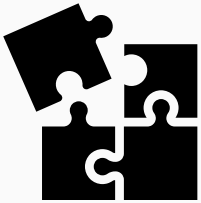
Combining Everything

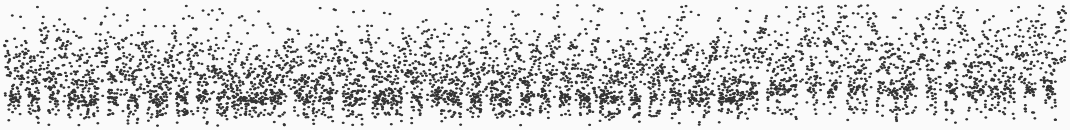


1. Use the counting primitive to measure DRAM accesses
2. Through the DRAM side channel, determine the row borders
3. Row borders have the 18 LSBs set to '0' $\rightarrow$ maps to cache set '0'
4. Build the eviction set for the Prime+Probe attack
5. Mount Prime+Probe on the buffer containing the multiplier

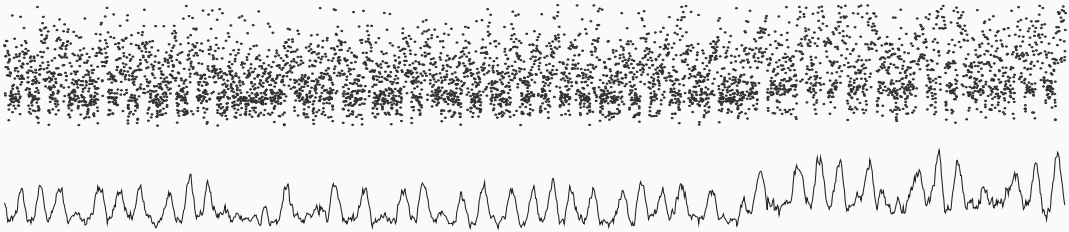
Results

Measured Trace

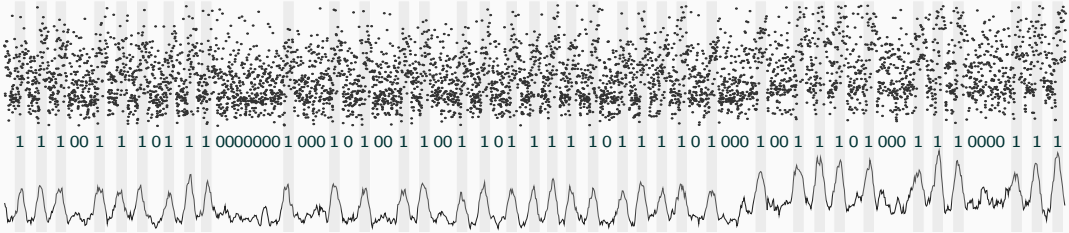
Raw Prime+Probe trace...



...processed with a simple moving average...

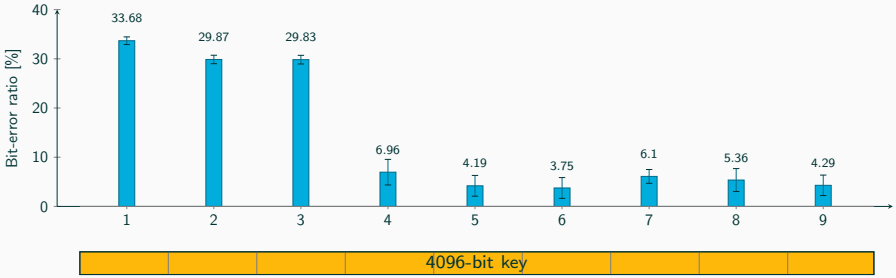


...allows to clearly see the bits of the exponent

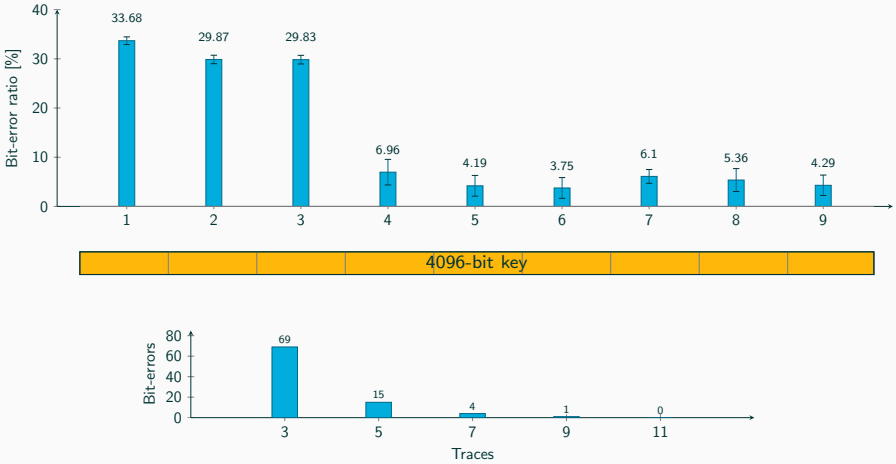


Error Probability

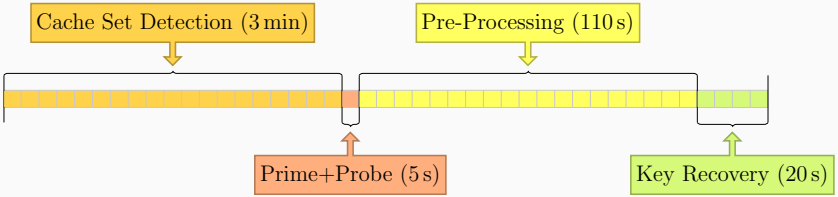
Error probability depends on which cache set of the key we attack



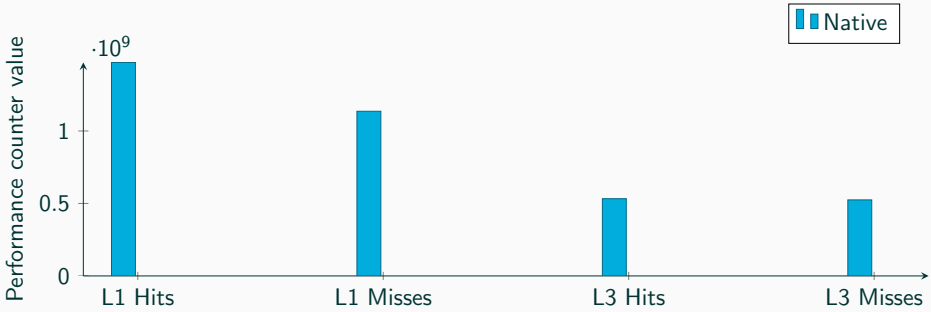
Error probability depends on which cache set of the key we attack



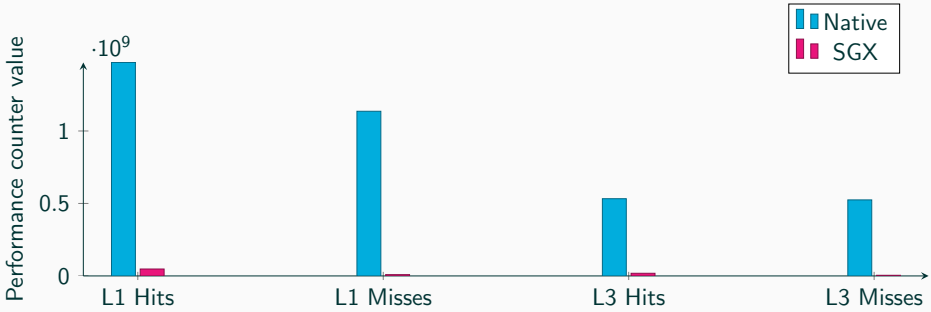
Full recovery of a 4096-bit RSA key in approximately 5 minutes



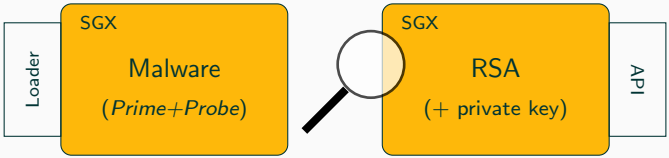
Performance Counters



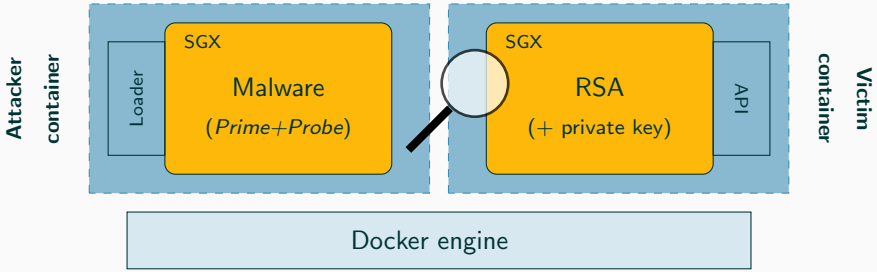
Performance Counters

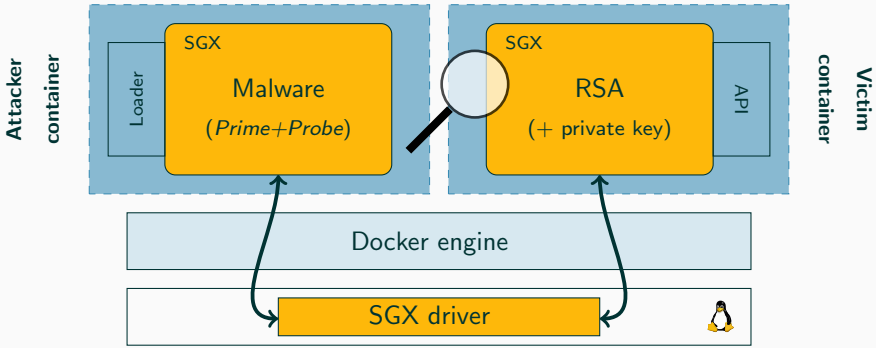


Bonus: Docker

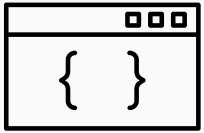


Bonus: Docker

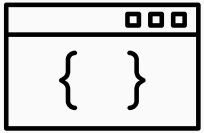



Attacker container
Loader
SGX
Malware
(Prime+Probe)
SGX
RSA
(+ private key)
API
Victim container
Docker engine
SGX driver

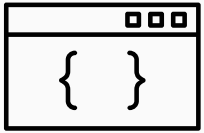
Countermeasures



- Cache attacks can be prevented on source level



- Cache attacks can be prevented on source level
- Use side-channel resistant crypto implementations



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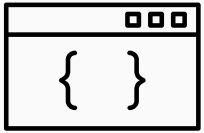

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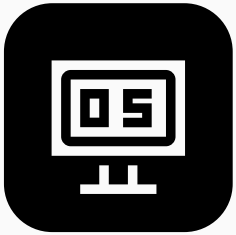

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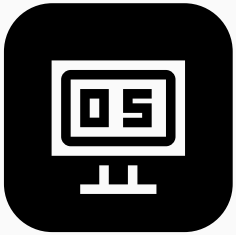

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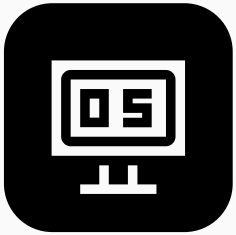

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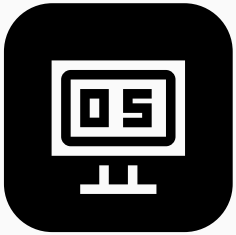

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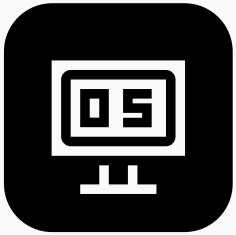

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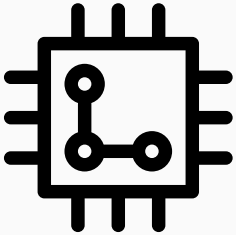
Hardware Level



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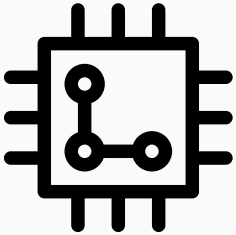

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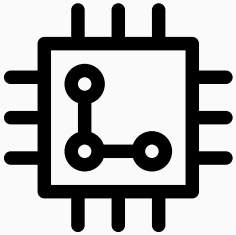

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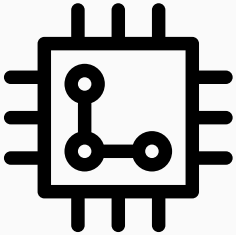

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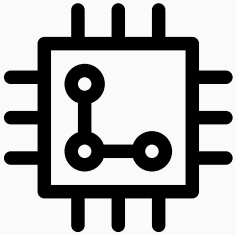

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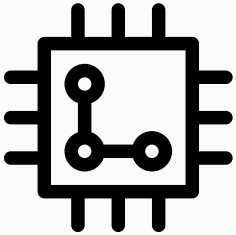

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- Provide a non-shared secure memory element which is not cached

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- Our end-to-end attack recovered 96% of a 4096-bit RSA key from a single trace, and the full key using only 11 traces
- SGX allows to completely hide an attack from state-of-the-art detection techniques
- The attack showed that SGX is not a magic solution to make software safe

Thank you!

Malware Guard Extension: Using SGX to Conceal Cache Attacks

Michael Schwarz, Samuel Weiser, Daniel Gruss, Clémentine Maurice, Stefan Mangard

July 6, 2017

Graz University of Technology